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IBM

Reference Manual

7750 Programmed Transmission Control

Preliminary Edition

PREFACE

This manual, a preliminary edition, presents the operation and use of the IBM 7750 Programmed Transmission Control. It provides a reference and guide for those familiar with the 7750 and serves as an instructional aid in the training of operators and programmers.

The 7750 Reference Manual contains four sections: Introduction, Detailed Description, Channel Adapters, and Communication System Design.

Section I introduces the 7750. It tells what the 7750 is, the computers that it can operate with, and how it functions in a TELE-PROCESSING® system.

Section II describes the 7750 functionally. This section covers in detail such areas as registers, timing, instructions, priority processing, and so on.

Section III explains the type of adapters used by the 7750 to communicate with the various terminals of a TELE-PROCESSING system. The description and operation of each type of adapter is presented.

Section IV tells the philosophy behind the design of the 7750, its flexibility, and its limitations. Tables are provides to show how various channel configurations are possible and practical.

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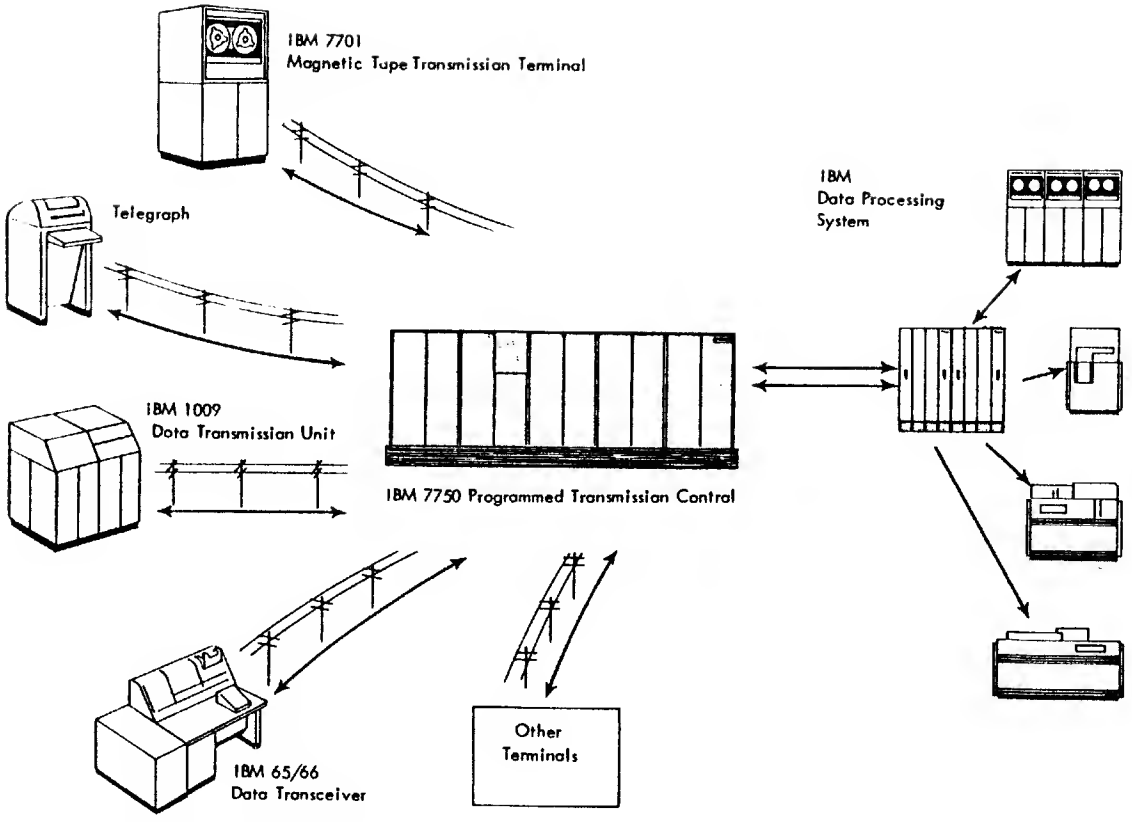


Figure 1. Communication-Based Data Processing System

INTRODUCTION

GENERAL INFORMATION

The IBM 7750 Programmed Transmission Control is a TELE-PROCESSING® system component that links a central computer with remote terminals. Tele-communications equipment such as telegraph terminals, IBM 65/66 Telegraph Data Transceivers, or IBM 7701 Magnetic Tape Transmission Terminals may be connected to the 7750 through appropriate channel adapters. On the other end, the 7750 is connected to an IBM Data Processing System through a data channel. The 7750 thus enables computer users to combine data processing capabilities with the transmission capacity of many telecommunication devices (Figure 1).

The 7750 is a stored program unit that serves as a buffer control device, directing and controlling the flow of information between the computer and its communication network. This communication network may have a variety of standard or specially designed terminals, each operating independently but linked directly to the system. The terminals may have different transmission speeds. The 7750 accepts electrical signals simultaneously from a number of communication lines, converts these signals into bits, then into characters, then into records and, finally, relays these records at high speed to the computer for processing.

In most uses, the prime function of the 7750 is to connect the diverse elements of the communication network to an associated computer such as the IBM 1410, 7040, 7044, 7070, 7074, 7080, 7090, or 7094. TELE-PROCESSING systems using the 7750 may be employed for airline reservations, message routing, centralized data processing, production control, or other applications. The system planner can choose the computer and be assured that the communication problem will not be a significant factor in determining his choice.

The TELE-PROCESSING system depends on the terminals used, which model of the 7750 is installed, and the traffic volumes of the customer.

Within a TELE-PROCESSING system, the 7750 performs five basic functions:

Data Assembly (and Distribution) proceed automatically with only occasional supervision from the stored program. Data assembly begins with the derivation of bits from the incoming communication circuit by the channel adapter. The process continues to the point where characters are assembled into complete data messages in the process storage section of the 7750.

Information Conversion from or to the form required by the computer may include changes to both the code and format of the message. Conversion is controlled by the 7750 stored program.

Editing involves omitting and adding special characters -- and, sometimes, format changes -- under program control.

Monitoring and Supervision checks incoming (or outgoing) traffic to indicate the status of terminals and oversees the data flow in a network. The stored program controls these functions.

Data Transfer supplies data to and accepts data from the computer, on a demand and response basis, through linkage connecting the 7750 and the computer.

GENERAL ORGANIZATION

The 7750 is made of five standard IBM racks. An optional sixth rack is used for low speed relay connection to telegraph lines.

1. Communications Line Terminator Rack

The major function of this rack is to aid the customer in isolating troubles in his communications network. The rack contains patch panels, signal generation circuitry, and equipment to aid in the running of diagnostic programs in the 7750.

2. Channel Adapter Rack

This rack is designed to hold different types of Channel Adapters, and different combinations of these types. The Channel Adapters perform a variety of functions such as time multiplexing a number of low speed communications channels into one high speed output, and recovering bit timings from synchronous data. The design of this rack is modular, to match different types of communications networks.

3. Process Control Rack

This rack contains the registers and the instruction control circuitry of the 7750. All processing is controlled by this rack.

4. Core Storage Rack

This rack contains two magnetic core memories, called Process Storage and Control Storage. Process Storage is available in three different sizes, 4,096, 8,192, and 16,384 words at 48 bits per word. Control Storage contains 128 words, 48 bits per word. The data and address registers for these storages are in the Process Control Rack.

5. Power Supply Rack

The Power Supply Rack contains all the power supplies necessary to run the 7750.

The IBM 7750 is organized around two magnetic core storages. Control Storage is used to control the communications network and to assist in the execution of the programs. This memory contains 128 words, 48 bits per word of storage. Process Storage is used to hold the message queues, and the programs. Process Storage may be one of three sizes; either 16,384 words, 48 bits per word; 8,192 words, 48 bits per word; or 4,096 words, 48 bits per word. The size of Process Storage is chosen to fit particular job applications. All important functions of the 7750 are performed in and around these memories.

COMMUNICATIONS TERMINOLOGY

The following communications terms are defined to clarify the explanation of 7750 operation.

Half Duplex -- A half duplex communications channel is one in which information can be transmitted in either direction, but only one direction of transmission may be employed at any one time.

Full Duplex -- A full duplex communication channel is one in which information can be transmitted in both directions simultaneously. In actual practice, full duplex channels are often made of two half duplex channels.

Start - Stop Transmission -- In this method of transmission the data bits are preceded by a start bit, and are followed by one or more stop bits. The total number of stop bits is not necessarily an integer. The purpose of this method is to allow the receiving terminal to stay in synchronization with the transmitting terminal. The start and stop bits are the synchronizing information, and thus the receiver is resynchronized by each character. This method of transmission is used by normal telegraph machines.

Synchronous Transmission -- In this method of transmission, the receiving terminal is initially synchronized with the transmitting terminal by the receipt of special synchronizing information, (bit pattern) and then the transmission of data begins. While data is being transmitted, no special synchronizing information is needed. It is assummed that both terminals will stay in step for the duration of the transmission. At intervals, new synchronizing information will be transmitted. This may be done at the beginning of every message, or it may be done as infrequently as once a day. Synchronous transmission is generally used on high speed channels, since one of its main advantages is that it requires less bits than start-stop to transmit the same amount of information. For example, the IBM 7701 Magnetic Tape Terminal employs synchronous transmission.

Sub-Set -- The word subset is an abbreviation for the words subscriber set. This is a modulation-demodulation device which accepts as an input binary-valued electrical signals, and gives as an output a modulated wave form, suitable for transmission over a communications channel. Conversely, the subset receives modulated wave forms from the communications channel and converts them into binary-valued electrical signal outputs.

ASSEMBLY OF CHARACTERS

Messages from the communications network enter the 7750 via one of several types of channel adapters. These adapters perform a variety of functions. One type, the Low Speed Group, time multiplexes a number of low speed communications adapters into one

high speed information channel. It does this by a process of scanning and storing the results in a small core buffer. The high speed adapter (HSA2) receives its information from an FM subset or the 202 A or B subset. All adapters communicate with Control Storage by means of the Adapter Control Interface.

Adapter Control Interface

The Adapter Control Interface connects the channel adapters to the Control Storage Data register. This interface contains nineteen lines. Each adapter is connected in parallel to these nineteen lines, and a sixteen position scanner selects a particular adapter at a given time. In other words, all the adapters are on a bus system, with the scanner doing the selecting. The scanner is timed sequentially; there is no addressing of the scanner and no priority scan system employed.

Three types of information are passed across the interface. They are: data, control information, and addresses. Data is transferred serially one bit at a time. Characters are not assembled in the adapters; they only acquire bits. Therefore, data is transferred one bit at a time across this interface, together with control information telling when a new bit should be accepted. Address information is transferred from the adapters to Control Storage, each adapter having one or more Control Storage locations associated with it. The rest of the control lines perform such functions as indicating to an adapter whether it should be in sending or receive status, or indicating to Control Storage when some type of error has occurred in the adapters. All the lines in the Adapter Control Interface are controlled by a word in Control Storage, called the Channel Word.

Channel Word

The Control Storage operates on two different types of cycles alternately. These cycles are called Scan and Process cycles. The Process cycle is devoted to message processing and is discussed later. The Scan cycle is devoted to receiving bits from, or transmitting bits to the communications network. During Scan cycles, Channel Words are read from Control Storage. The address of this word is generated in the channel adapter selected by the sixteen position scanner in the Adapter Control Interface. There is at least one Channel Word per half-duplex communications channel connected to the 7750, and two Channel Words for each full duplex communications channel attached; one word for the receive portion of the full duplex channel, and one word for the transmit portion of the full duplex channel. These channel words completely control the action of the associated communications channel.

The Channel Word has three major functions: It serves as the assembly area in which bits are assembled into characters; it directs the assembled character into the proper queue, and it controls the communications channel.

1. The assembly of bits into characters is done in one 11 bit field of the 48 bit Channel Word. Character length may be any number of bits from one to eleven. As this

assembly field is a shift register, bits are accepted one at a time and shifted until a complete character has been received. During transmission, a complete character is put into the assembly area, and shifted out one bit at a time. Certain control fields are associated with the character assembly field. These are the Character Length and the Bit Count. The Character Length is a four bit field used to indicate the size of the character being received or transmitted over this particular communications channel. The Bit Count is a four bit field which may be used to indicate how many bits of a given character have been received or transmitted. The use of these fields differs somewhat in start-stop and synchronous transmission, and their exact usage is explained in the detailed description section. As an example, however, consider the reception of a synchronous transmission which uses six-bit characters. To do this the Character Length would be set to six by the program, and the Bit Count would advance every time a bit was received. Every time the Bit Count equalled the Character Length, a complete character had been received. Three fields, the character assembly field, the Character Length, and the Bit Count, working in conjunction with one another, allow the reception and transmission of variable character lengths, one bit at a time.

2. When the character has been assembled, it must be directed into the proper queue in Process Storage. Another field in the Channel Word contains a 16 bit address which refers to Process Storage. The assembled character is stored at this location in Process Storage. Note that 16 bits are sufficient to refer to 65,536 locations. Each word in Proccss Storage may be divided into four fields, and the address in the Channel Word is sufficient to specify any of them. When the character is complete, it is immediately put into Process Storage, regardless of what else may be going on in the machine. This process of transferring a complete character from the Channel Word to the Process Storage is called Character Interrupt, and is done automatically without program intervention. After a character has been transferred to Process Storage, the 16 bit address in the Channel Word is automatically incremented by one. When transmitting, the reverse procedure takes place. Characters are transferred from Process Storage into the character assembly field of the Channel Word, and the address in the Channel Word is incremented.

3. The third function of the Channel Word is to control the communications channel. A number of bits in the Channel Word are used for this purpose. These bits perform such functions as indicating whether the channel is in send or receive status, whether the start-stop or synchronous mode of transmission is being used, whether the initial synchronization pattern has been found, or whether the channel should be searching for this pattern, and whether the 7750 is waiting for a response on this channel. The use of these bits in the Channel Word are further explained in the next section.

By assigning these functions to the Channel Word, and by having at lease one Channel Word per communications channel, it is possible to have every communications channel operating in a different fashion, using different character lengths, and different methods of transmission, and yet maintain control over the channel by accessing the proper word. Only one control register is required, the Control Storage Data Register and it is time shared. Thus, the Channel Word concept provides an economical means of channel control and of character assembly.

Qucue Formation

When characters have beeu assembled in Channel Words, they are automatically transferred into a queue in Proeess Storage. The formation and maintenanee of these queues is one of the most important tasks performed by the 7750. A large portion of Process Storage may be oeeupied with sueh queues sinee there will be an incoming queue for every channel reeeiving information from a eommunication terminal, an outgoing queue for evcry channel transmitting information to a eommunication terminal, a queue of information for the eomputer, and a queue of information eoming from the computer. If Process Storage is to be effieiently used, a good system for assigning queuing space must be used.

Many methods of memory spaee assignment are possible. For example, a fixed bloek of storagc ean be assigned to each eommunications channel for its queuing spaee. This is a relatively inflexible and ineffieient method of storage loeation. Problems exist of overflowing tlie fixed amount of spaec, or of never using an appreeiable fraction of the spaee. Tlie problem is made more severe sinee message lengths are not restricted or in any way eontrolled. Tlie 7750 assigns its memory space for queues by the proeess of chaining.

Chaining eonsists of assoeiating a suffieieut number of pieees of memory spaee so that enough storage loeations are available to perform a given job. For purposes of chaining, Proeess Storage is broken into pieees called bloeks. Each block consists of 8 words. Each word is broken into four fields of eleven bits each. Therefore, thirty-two characters may potentially be stored in eaeh block. However, the thirty-second storage loeation in each bloek is reserved for a speeial eharacter, ealled the Block Control Charaetcr. Eaeh block has a starting address whose five low order bits are all ZERO'S, and since there are thirty-two characters per bloek, an ending address is one whose five low order bits are all ONES.

The Block Control Charaeter is the means by which the bloeks are ehained together. The Block Control Charaeter is tlie 11 high order bits of the starting address of the next block in the ehain. For example, four bloeks ean be arbitrarily labeled A, B, C, and D. Figure 2 shows these blocks with their starting addresses. Figure 3 shows these bloeks chaiued together, the order of the chain being C-A - B-D. They are chaiued beeause tlie Bloek Control Character in block C is the eleven high order bits of the starting address of block A; the Block Control Character is block A in the eleven high order bits of the starting address at block B, and so on. By means of chaining, small pieces of storage have been effeetively assembled into a larger portion of storage. Note that tlie bloeks whieh make up the ehain are not neeessarily continuous in storage. These blocks may be physieally located almost anywhere within Proeess Storage, but they aet like a eontinuous segment of storage due to chaining.

To make this proeess work, a eertain amount of bookkeeping is required. One method of doing this is as follows: First, ehain together all the unused bloeks of memory. Then maintain as reeords two addresses, A1, the starting address of the first empty bloek in tlie chain, and A2, the address of the Block Control Character in the last empty

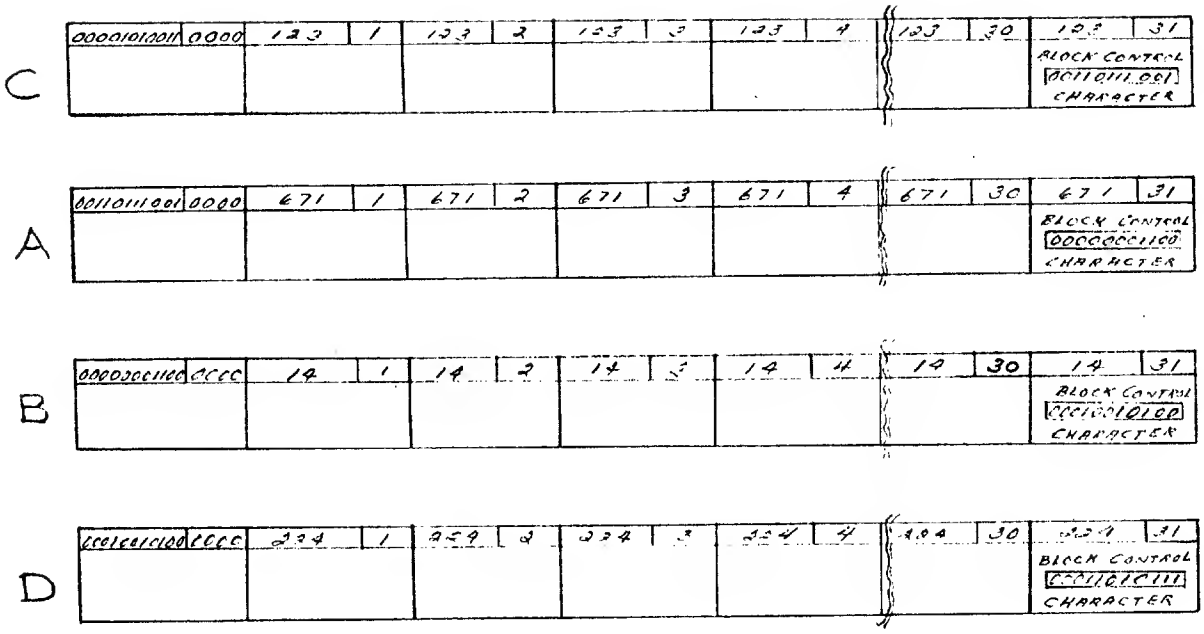


FIGURE 2 BLOCKS

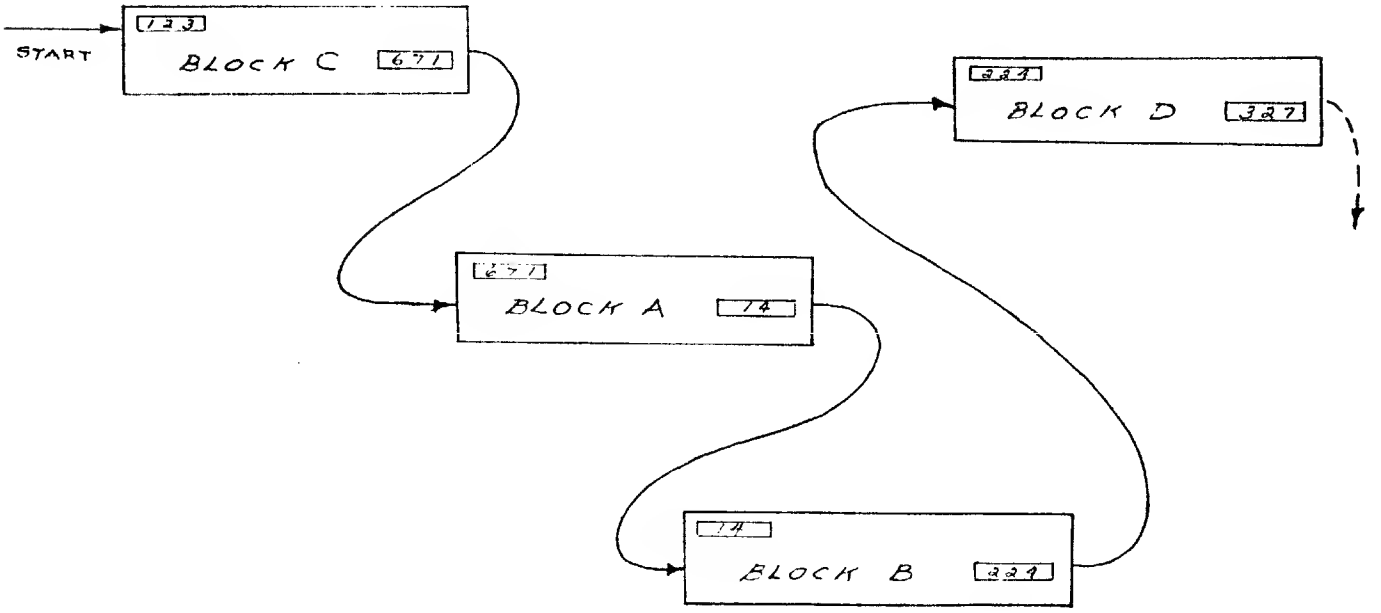


FIGURE 3 CHAIN C-A-B-D

block in the chain. Suppose that a message queue has filled its chain and that another block is required. Then the eleven high order bits of the starting address of the next block are put into the Block Control Character of the last block in the message queue, and the first empty block from the chain of empty blocks is attached to the message queue. Since this block is chained to the rest of the empty blocks, its Block Control Character is the starting address, A3, of the next empty block in the chain. Now A3 should be stored in the location which formerly held A1, since A3 is now the starting address of the first block in the chain of empty blocks. Thus, the process can be repeated.

When blocks become empty they must be returned to the chain of empty blocks. Suppose that A4 is the starting address of an empty block which is to be returned to the chain of empty blocks. A4 is then written at the address specified by A2. In other words, A4 is written as the Block Control Character of the last block in the chain of empty blocks The block whose starting address is A4 is now connected to the end of the chain of empty blocks. To complete the process, A5, the address of the Block Control Character of this block, is now written in the location at which A2 was stored.

After both these operations have been completed, a block has been removed from the front of the chain of empty blocks, and a block has been added to the end of the chain of empty blocks, and the addresses A3, and A5 have been stored. These addresses are again the starting address of the first empty block in the chain of empty blocks, and the address of the Block Control Character of the last block in the chain of empty blocks.

In the 7750, the chaining process is done under program control. When a particular channel requires more storage space for its queue, the Channel Service program is automatically brought into operation. The need for this program is sensed by noting when the five low order bits of the address contained in the channel word are all Ones. This indicates that the end of a block has been reached and that Channel Service is necessary to assign a new block to the chain. Thus far, characters have been assembled, and put into queues in Process Storage. They will next be processed in some way before being sent on to the computer.

MODE SYSTEM OF INTERRUPTS

The 7750 works in an essentially uncontrolled environment. In many applications, the 7750 cannot dictate when messages will occur on the communications network, or what the length of these messages will be. Communications from the associated computer may take place at random intervals. For these reasons, the 7750 is equipped with a very flexible interrupt system, so that it may quickly and automatically switch from one program to another when various conditions require immediate attention.

This interrupt system has several levels. An interrupt may interrupt an interrupt, and so on. Priorities are assigned to various classes of interrupts so that the machine can decide which interrupt to execute. There are six such classes of priorities in the 7750, and these classes are called modes. These modes, listed in order of decreasing priority are:

1. Service
2. Channel Service
3. Copy
4. Out
5. In
6. Normal

At the end of every machine cycle, the mode circuitry is examined to determine what modes are requested. The machine will then go into the requested mode with the highest priority and execute the programs associated with that mode. Requests for a mode are stored in a particular register, called the Mode request Register. This register maintains the requests until they can be serviced.

For example, assume the 7750 were in Normal Mode, and that some error detection circuitry turned on the Service Mode request, and during the same cycle the request for Channel Service Mode was turned on. The 7750 would then automatically start to execute the Service Mode programs, and when it had completed this program, it would switch into Channel Service Mode, and execute the Channel Service program. Finally, if no other mode requests had occurred, the 7750 would fall back into Normal Mode, and continue to execute the normal mode program from the point of the interruption. Note that a new mode may be requested either by the program, or automatically by means of special hardware.

Changes in mode can be made without any special preparation on the part of the programmer. It is not necessary to write a number of housekeeping programs to change modes. Instead, the 7750 stores all working registers and the instruction counter at the end of every machine cycle. Instruction counters are stored in Control Storage in a special format called the Process Word, or P word. This word contains three working registers as well as the instruction counter. There is one P word for each mode. Therefore, to change modes it is only necessary to access a different P word in Control Storage. The instruction counter in this P word will then address the programs associated with the new mode.

METHODS OF PROCESSING

The 7750 processes messages in real time, in a wide variety of formats, character sizes, and codes. Methods of processing must be extremely flexible to meet the diverse requirements. Therefore, table look-up is the fundemental processing technique.

Table look-up is used for many purposes in a typical 7750 program including Code translations. Any code of up to 11 bits per character may be readily translated into any other arbitrary code of up to 11 bits per character. All shifts are performed by using shift tables. There is no shift instruction. Arithmetic operations are performed by means of multiple table look-ups. Perhaps the most important use of this technique is to control the operation of the Normal Mode program.

As an example of how the program may be controlled by table look-up, consider a telegraph polling system in which five programs may be required. These programs are Polling, Sending Data, Answer Back, Header Processing, and Message Processing. Assume there are 20 telegraph channels connected to the 7750. Each channel will require these programs in unpredictable sequence. A technique for handling this situation requires the use of a Program Branching Table, and the assignment of a unique identification number, called a Channel Number, to each communication channel. The 7750 then uses the Channel Number to address the Program Branching Table. The Program Branching Table will then cause the program to branch to the proper one of the five programs. The last action any one of the programs performs is to update the relevent entry in the Program Branching Table so that the next time the Table is addressed by the Channel Number, the proper program will be selected.

Table look-up operations can be programmed, due to certain features of the instruction set. These features are an address modification method, and a register and size specification method. Each method is described below.

The 7750 is a single address machine. In many instructions, this address can be modified by means of information specified in the instruction. Two fields in an instruction, the M field and the L field, specify this modification. The M field specifies a particular register, and the L field specifies from zero to eleven low order bits in that register. These bits then replace the L low order bits in the address before the instruction is executed.

Consider as an example, an instruction containing the address $(163245)_8$; with M specifying the Y register, and L equaling 5. Assume the contents of the Y register to be $(3732)_8$. The instruction would then be executed as though the address it contained were $(163272)_8$; that is five low order bits of the Y register have replaced the five low order bits in the instruction.

The register and size feature of the 7750 instruction set allows the results of many machine instructions to be placed in one of seven addressable registers. The particular register to be used may be selected by setting the proper bits in the R field of the instruction. The number of bits which are to be loaded into the specified register may also be varied by setting the S field of the instruction. This feature allows the programmer to have the option of loading from zero to eleven bits into the specified register.

The combined use of the register and size feature, and the address modification method allows a table look-up to be performed in one instruction, with the final result stored in a designated register.

The instruction set contains other useful features. These features include the ability to perform most instructions with an indirect address; the ability to complement the operands in an instruction and the ability to increment the address of the Process Storage word address by the instruction. Indirect addressing, complementing, and incrementing may be done individually, or they may be done in combination when executing most instructions.

The instruction set makes message processing more efficient. The program operates upon characters and messages which have been automatically stored in the Process Storage. There will be one queue of data to be processed for each receiving communications channel, and one queue of data to be processed from the computer. The program processes the contents of these queues, character by character, and places the results in other queues. Some of these queues will be transmitted back into the communications network, and one queue will be transmitted to the computer. Thus information has been acquired from the communications network, processed, and is now in the format which the associated computer requires.

INFORMATION TRANSFER

The 7750 connects to a host computer by a read bus, a write bus, and a number of control lines to the proper data channel. The 7750 can be connected to the IBM 1410, 7040, 7044, 7070, 7074, 7080, 7090, and 7094 data processing systems.

The 7750 operates in three modes to service the computer. These modes are In, Out, and Copy. The In mode is used to prepare the 7750 for receipt of information from the computer. The control lines are examined, and the proper responses are made. The In mode program prepares a block of storage for the incoming information and sets up the proper control word so that the 7750 can determine when all the information has been received from the computer. The Out mode is used to prepare the 7750 for the transmission of information to the computer. Its mode program sets the proper signal to inform the computer that the 7750 has information to transmit. In addition, this mode program also prepares the queue of outgoing information, and sets up a control word so that the 7750 can determine when all information has been sent to the computer.

The actual transfer of information takes place in Copy Mode, which has no program. Information is transferred one character at a time, using a demand and response system. The control words which were prepared in the In or Out modes terminate character transfer at the proper number.

DETAILED DESCRIPTION

PROCESS STORAGE

The IBM 7750 Process Storage is a magnetic core storage available in three sizes:

4,096 words
8,192 words
16,384 words

Each word contains 48 bits, including one parity bit.

Process Storage Word Formats

The contents of a word in Process Storage may be arranged in several ways, depending upon its intended use. Figure 4 shows the word format for Data Words, Instruction Words, and Limit Words.

Data Word - DWD

The Data Word is made up of four eleven-bit registers; A, occupying bit positions 47 through 37; B, occupying bit positions 33 through 23; C, occupying bit positions 22 through 12; and D, occupying bit positions 11 through 1. Bit positions 36 through 34 are not used. Bit position P is the parity bit for the entire word.

Instruction Word - IWD

The Instruction Word contains a ten-bit Operation Code in bit position 1 through 10, an OP code parity bit in bit position 11, a two-bit Flag field in bit positions 12 and 13, a four-bit L field in bit positions 14 through 17, a three-bit M field in bit positions 18 through 20, a four-bit S field in bit positions 23 through 26, a three-bit R field in bit positions 27 through 29, and a 16-bit Address in bit positions 32 through 47 (low order in position 32). Bit position P is a parity bit for the word, and bits 21, 22, 30, and 31 are not used.

Limit Word - LWD

The Limit Word, shown in Figure 4, contains a 16-bit address in the normal Address portion of the word (W). The Address occupies bit positions 32 through 47 of the word. In addition, the word contains a Limit of 16 bits which fills the C, and part of the B character fields. The five low order bits of the Limit occupy bit positions 23 through 27 in the B character field.

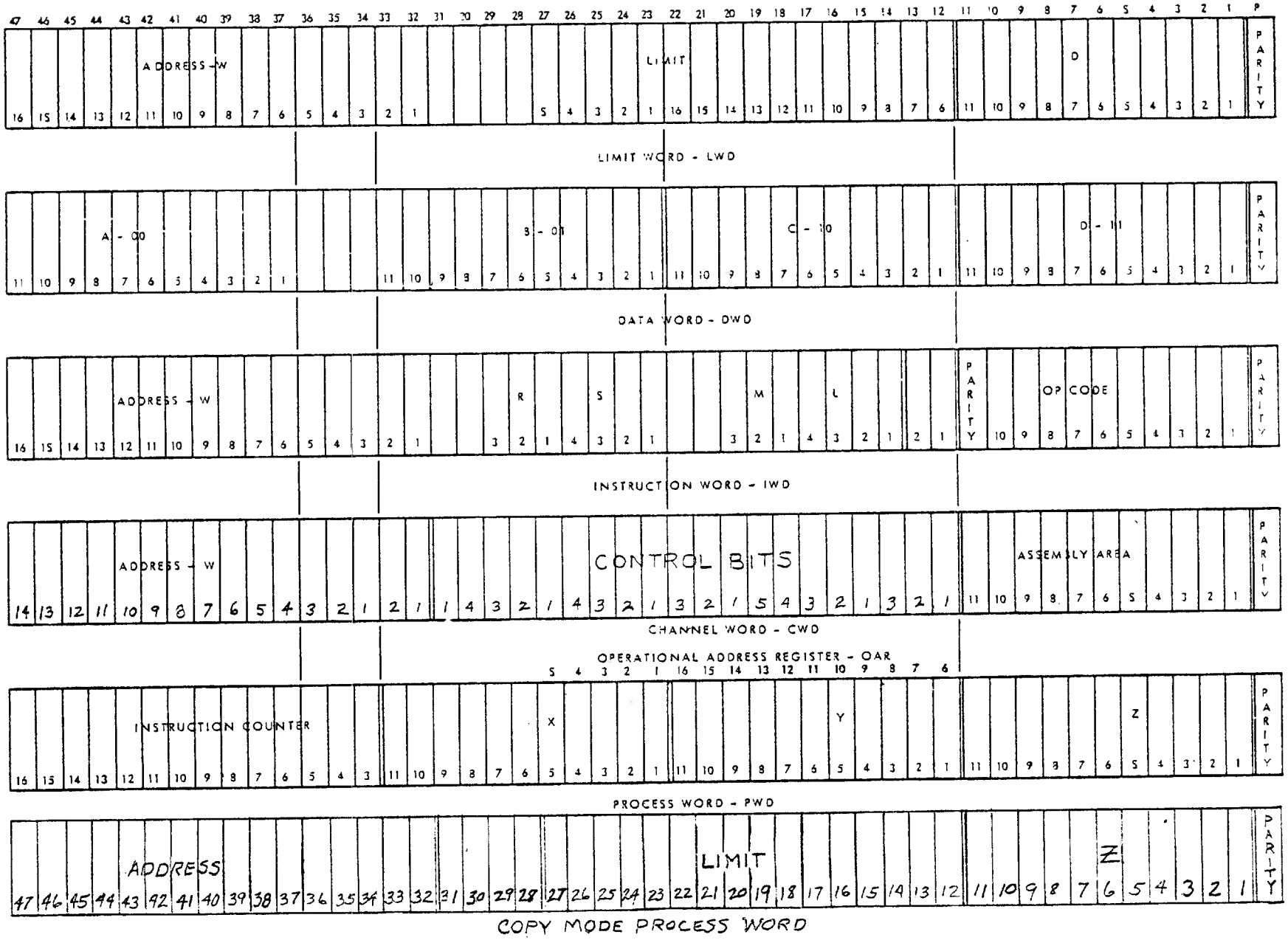


FIGURE 4 IBM 7750 WORD FORMATS

CONTROL STORAGE

The IBM 7750 Control Storage is a magnetic core storage with a capacity of 128 words. Each word has 48 bits, including one parity bit.

The Control Storage operates on alternate Scan and Process cycles of 11 microseconds and 17 microseconds, respectively. The Scan cycle contains 3 microseconds for modification of the data word between read and write, and the Process cycle contains 11 microseconds modification time. The beginning of the Control Storage Scan cycle precedes the beginning of the Process Storage Instruction cycles by 6 microseconds.

Data is entered into and out of the Control Storage by means of the Control Storage Data Register (CSDR).

Control Storage Data Register

The Control Storage Data Register is a 48-bit register which holds the word to be read out of, or to be written into storage. See Figure 4. The control circuits for this register provide the means to use it as:

(1) a single 48-bit register.

(2) four independent registers; X, Y, Z, (which are 11 bits), and an Instruction Counter (which is 14 bits).

(3) three independent registers; Z (which is 11 bits), an Operational Address Register, and an Address of 16 bits each.

The Z register is a count down counter which may be decremented under program control.

Control Storage Word Formats

The Control Storage Word will be arranged in three ways, depending upon its intended use. These word formats are described below. See Figure 4.

Channel Word - CWD

The Channel Word is divided into fields as indicated in the following table:

Field	CSDR Position No.
W - Word Address	47-34
A - Character	33-32
B - Last Timing	31
C - Character Length	30-27
D - Status-Micro	26-23
E - Action	22-20
F - Character Control	19-15
G - Status-Macro	14-12
H - Assembly/Distribution	11- 1
P - Word Parity	P

Process Word - PWD

For all modes except the Copy Mode, the Process Word will have one of the following interpretations:

Field Name	No. of Bits	Position
Instruction Counter	14	47-34
X	11	33-23
Y	11	22-12
Z	11	11- 1
Word Parity	1	P

or

Instruction Counter	14	47-34
Operational Address Register	16	27-12
Z	11	11- 1
Word Parity	1	P

The second interpretation is used only with the Address and Limit moving instructions.

Copy Mode Process Word

During the process cycle of the Copy Mode, the Control Storage Data Register is interpreted as follows:

Field Name	No. of Bits	Position
Address	16	47-32
Limit	16	27-12
Z	11	11- 1
Word Parity	1	P

REGISTERS

Registers are temporary storage devices. The size of a register is determined by the number of bits of information it can hold. Its use is determined by the nature of information that goes into the register. For example, a data register temporarily stores data, an address register temporarily stores an address, an instruction register temporarily stores an instruction, and so on.

From the programmer's point of view, registers may be divided into two general types: addressable and non-addressable. Addressable registers can be addressed by the stored program. That is, an addressable register may be loaded, set, or requested by the programmer.

Non-addressable registers cannot be addressed by the stored program. They are set and reset automatically at the proper time. Figure 5 shows the registersof the 7750.

Non-Addressable Registers

Instruction Register

The Instruction Register is a 26-bit register which holds all of the instruction being executed, except the address. The first 10 bit positions contain the OP Code, the next two bit positions contain the Flag bits, the last 14 bits contain the R, S, M, and L fields.

Mode Status Register

The Mode Status Register is a 5-bit position register. Before the execution of each instruction, this register selects the bit associated with the highest priority mode from the priority requests contained in the Mode Request Register. At any one time, the Mode Status Register may contain only one bit (a logical One) to indicate the highest priority mode selected. If this register contains no logical One, the 7750 selects the Normal Mode.

Process Storage Address Register #1

The Process Storage Address Register #1 (PSAR #1) contains the current address for addressing the Process Storage. Address modification takes place as the address is set into this register from the Process Address Register #2 (PSAR #2). This register can hold 16 bits; fourteen bits are used to address the correct word in storage, and two bits are used to specify a particular character (0, 1, 2, or 3) within a four-character word.

Process Storage Address Register #2

The Process Storage Address Register #2 (PSAR #2) temporarily store a 16-bit address from the PSDR or CSDR. The address is transferred to the PSAR 1 when it is used to address the Process Storage.

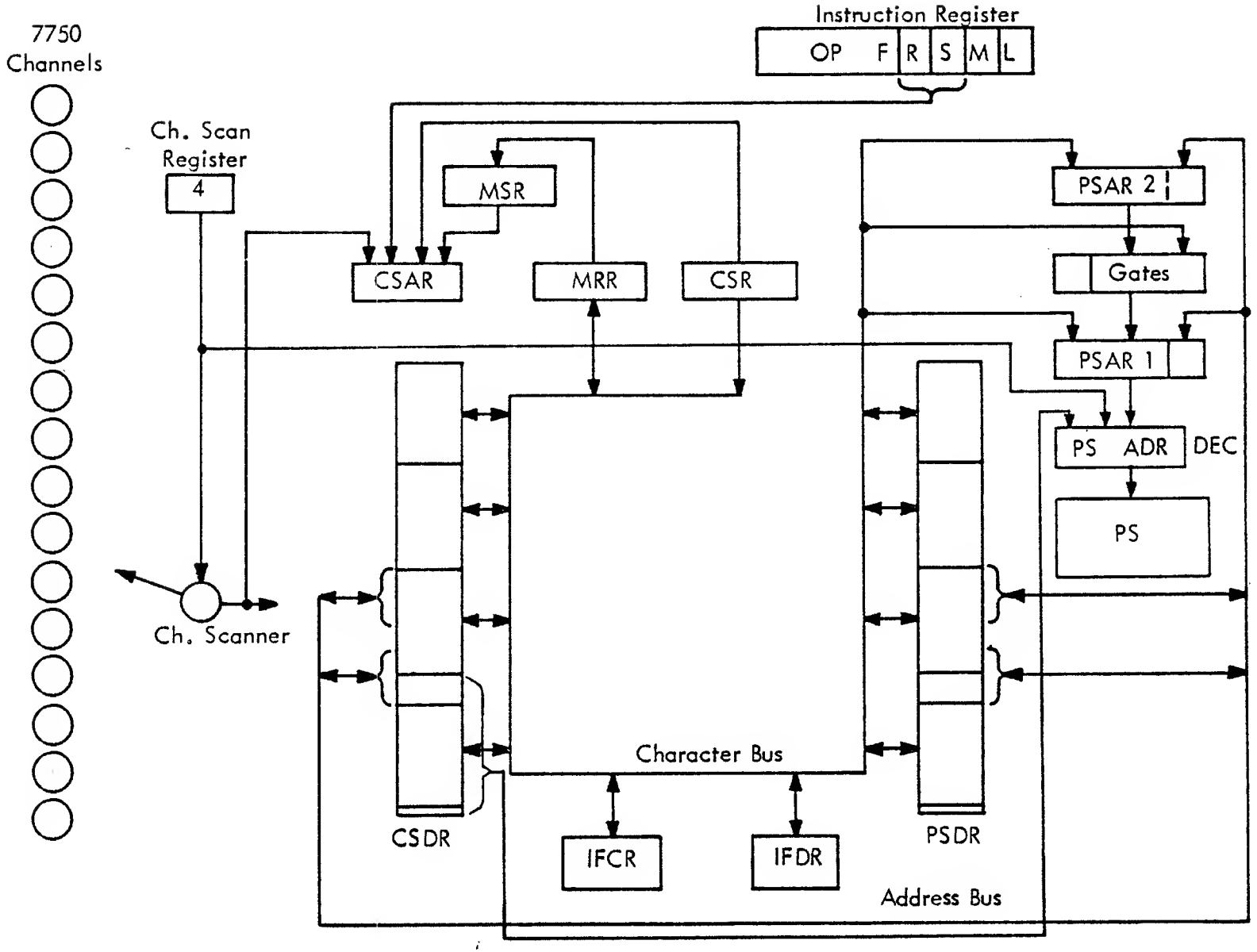


FIGURE 5 IBM 7750 REGISTERS

Control Storage Address Register

The Control Storage Address Register (CSAR) contains the current address for addressing a Channel Word or Process Word in Control Storage.

Process Storage Data Register

The Process Storage Data Register is a 48-bit register which holds the word read out from or to be written into Process Storage. This register can conform to any one of the three word formats in the Process Storage; namely, the Data Word format, the Process Word format, and the Instruction Word format.

Control Storage Data Register

The Control Storage Data Register is a 48-bit register which holds the word read out of or to be written into the Control Storage. This register can conform to any one of the four formats of the Control Storage; namely, the Channel Word format, the two Process Word formats and the Copy Mode Process Word format.

Addressable Registers

Channel Service Register

The Channel Service Register enables a channel requiring assignment of new storage space to identify itself to the Channel Service Program. This register has seven bit positions to hold the channel address. When Channel Service is obtained during a Character Interrupt or a Scan Cycle, the Channel Service Register is automatically set with the channel address.

During the execution of Storage-to-Storage instructions while in the Channel Service Mode, the 7750 transfers the contents of the Channel Service Register to the Control Storage Address Register to address Control Storage. This transfer is automatically done on the Second Process Cycle of a two cycle instruction which refers to the Control Storage while the machine is in Channel Service Mode.

Interface Data Register

The Interface Data Register is a nine-bit position register (eight bits plus one parity bit) which enables the 7750 to communicate with a computer. This register may be automatically loaded or its content stored under program control. It may also be loaded or its content automatically stored when data is transferred to or from the associated computer.

Interface Control Register

The Interface Control Register, an eight-bit register (Figure 6), controls the data flow between the IBM 7750 and the associated computer. This register may be loaded, its content stored or modified under program control. Most of these bits may be set or reset automatically when the 7750 is transferring data to or from the associated computer.

Mode Request Register

The Mode Request Register is a five-bit register which holds requests for priority program service (Figure 7). The 7750 requests a mode by setting the bit associated with that mode in the Mode Request Register to a logical One. A mode's priority depends on the position of its associated bit in the Mode Request Register. If more than one modes are requested in the Mode Request Register, the 7750 will always select the highest mode first. If no mode is requested in the Mode Request Register, the 7750 will execute the Normal Mode program.

TIMING

The basic machine cycle of the 7750 is 28 microseconds. Most 7750 instructions are one-cycle instructions. Two-cycle instructions, which require 56 microseconds for execution, are the instructions used for indirect addressing, with the exception of branch indirect, and storage-to-storage data manipulations.

For Control Storage operations, the basic machine cycle is divided into two storage cycles, scan and process, which are 11 microseconds and 17 microseconds long, respectively. During 7750 operation, the Control Storage goes through alternate cycles during which it:

1. Services one of the channels, assembling bits until a character has been accumulated, or sending bits until a complete character has been sent.

2. Provides the operational registers for the process storage to execute the instructions.

For Process Storage operations, the basic machine cycle is also divided into two cycles. These two cycles, the Instruction cycle and the Execute cycle, alternate and are 12 and 16 microseconds long, respectively. During an Instruction cycle, the 7750 obtains an instruction; during the execute cycle, it executes the instruction.

The Control Storage and the Process Storage cycles overlap, allowing the information of either cycle of either storage to influence the operation of the other. In one machine cycle the Process Storage goes through an Instruction cycle and an Execute cycle while the Control Storage goes through a Scan cycle and a Process Cycle. The Process cycle of the Control Storage, being 17 microseconds long, overlaps the Instruction and Execute cycles of the Process Storage.

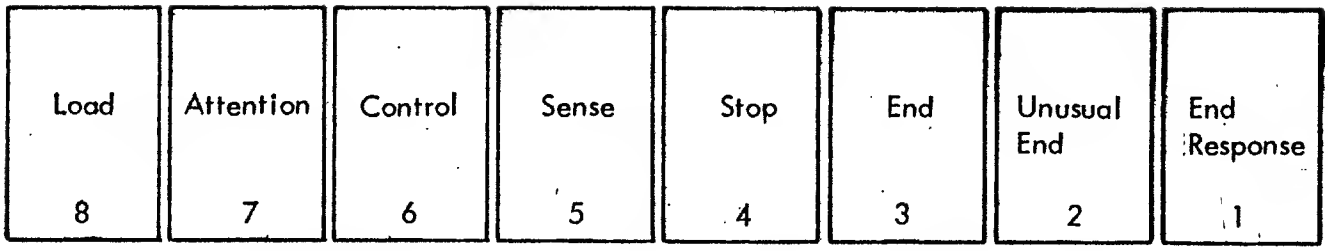


FIGURE 6 INTERFACE CONTROL REGISTER

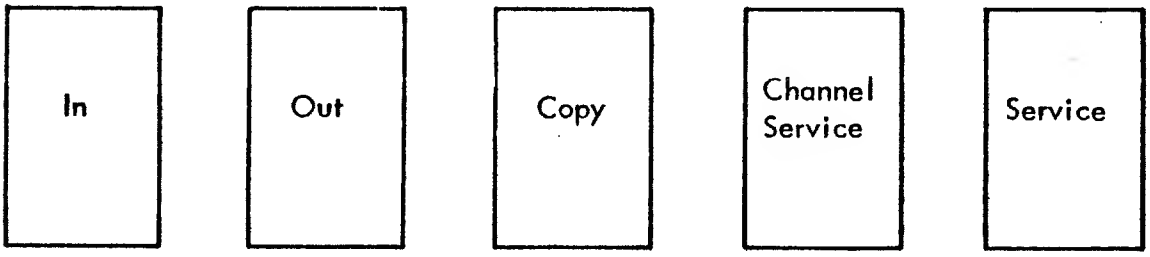


FIGURE 7 MODE REQUEST REGISTER

Clock Phases

The 7750 clock is composed of a 28 stage ring driven at a one megacycle rate. The clock cycles are divided into six phases, as shown in Figure 8. Four phases are used for single cycle instructions, and all six are used for two-cycle instructions. During phase one, the 7750 brings out an instruction from Process Storage, places it in the Instruction Register, and decodes it. During phase 2, the address contained in the Instruction Word is placed in PSAR #2. Later in phase two, if there is no address modification, the address in PSAR #2 is transferred to PSAR #1 to address the Process Storage at the beginning of the Execute Cycle. If there is address modification, the eleven low order bits of the address are modified as the address is transferred from PSAR #2 to PSAR #1. The location and length of the modifier is given by the M and L fields of the Instruction Word. Modification is accomplished by replacing the L low order bits of the address with L low order bits from the register specified by the M field. The modified address is used to address the Process Storage at the beginning of the Execute cycle. During a Branch on Zero or a Branch on Ones instruction, address modification cannot take place. This is because phase 2 is used to test S low order bits of Register R for zero or ones to determine if the branch takes place rather than used for address modification. The uses of phase 3 through phase 6 are determined by the types of instruction being executed.

One-Cycle Instructions

During phase one, the 7750 brings out an instruction from Process Storage, places this instruction in the Instruction Register and decodes it (Figure 8). At the beginning of the phase 2, the address contained in this instruction is placed in PS AR #2, then moved into PS AR #1 for addressing Process Storage. At the end of phase two, the instruction counter is incremented to address the next instruction at the beginning of the next machine cycle. If the instruction being executed is a skip type instruction, the instruction counter will be incremented again in phase 3. The use of the remainder of phase 3 and phase 4 depends on the type of one-cycle instructions to be executed.

Branch Instructions

At the beginning of phase 2 of a non-indirect branch type instruction, the Address contained in the Process Storage Data Register is not moved to PSAR #2. Therefore, the Process Storage Address is not addressed during this phase. In phase 3, this Address is placed in the Instruction Counter of the Process Word contained in the Control Storage Data Register. During phase 4, the Instruction Counter is put in PSAR #2 and later moved to PSAR #1 to address Process Storage. At some time in phase 4, the Instruction Word is read back into Process Storage and the Process Word is read back into Control Storage.

At the beginning of phase 2 (Figure 9) of an indirect branch type instruction, the address contained in the Process Storage Data Register is placed to PSAR #2. This Address is then shifted from PSAR #2 to PSAR #1. The remaining part of the cycle is used in the same manner as described above for non-indirect branch type instructions.

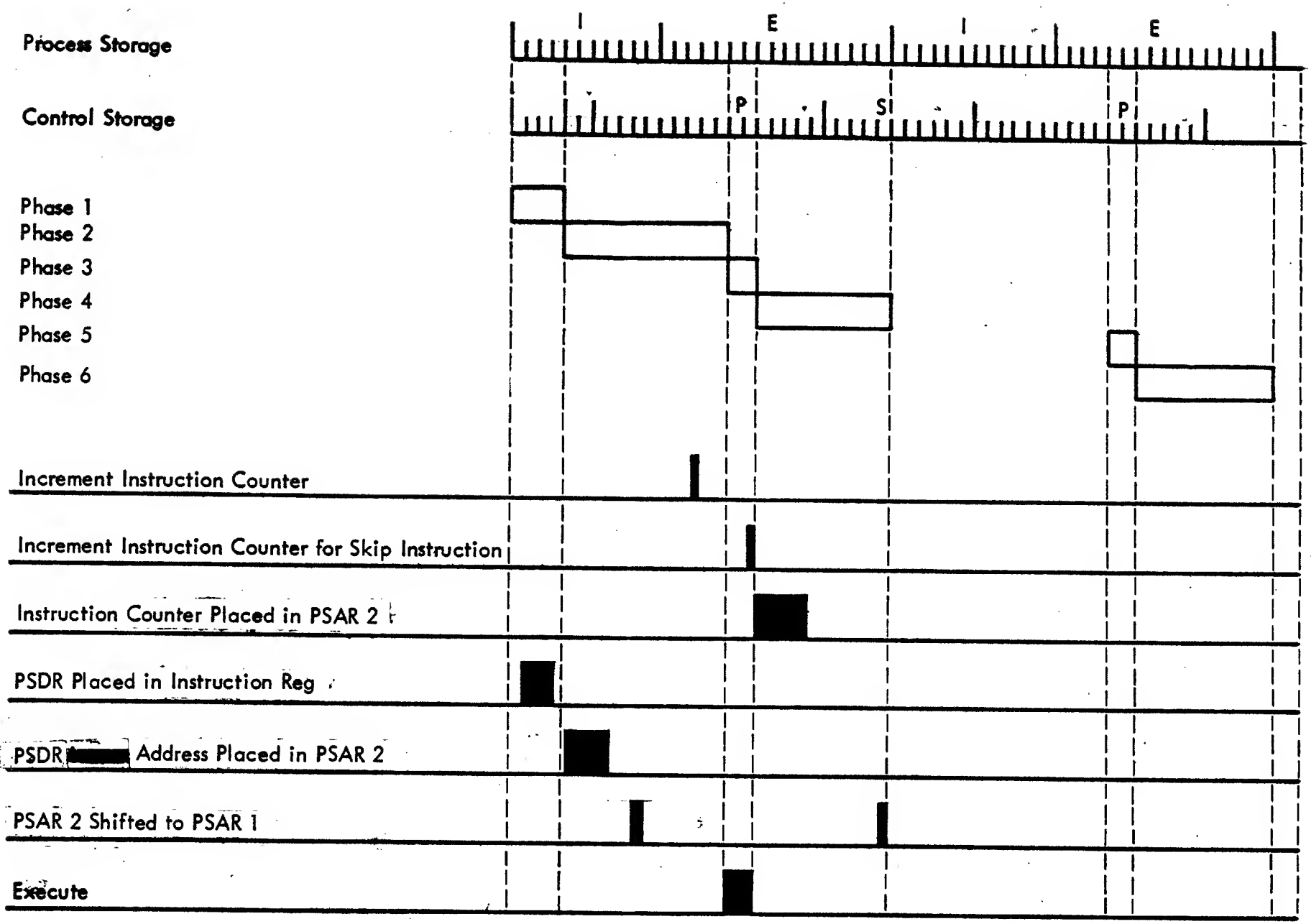


FIGURE 8 ONE CYCLE INSTRUCTIONS

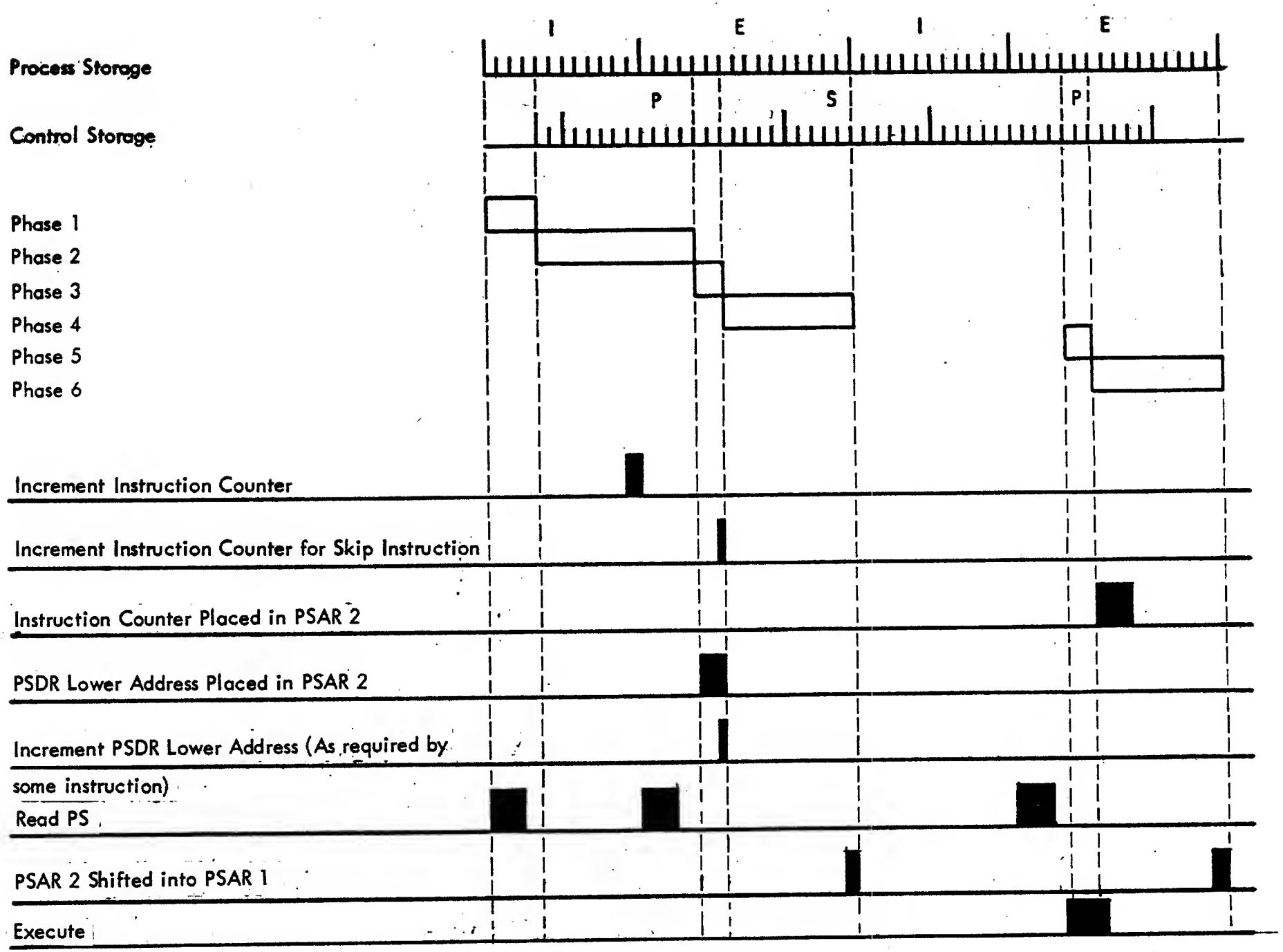


FIGURE 9 INDIRECT INSTRUCTIONS

Compare Address to Limit

During phase 3 of this type of instruction, the Limit of the Process Storage Data Register is compared with the address. If they are identical, the 7750 takes the next instruction in sequence. If they do not compare, the Address is incremented. During phase 4, the Instruction Counter is placed in PSAR #2 and the data registers are stored.

Character and Address Moving Instructions

During phase 3 of a character or address moving instruction, the character or address is placed in the proper register such as the OAR or the PSDR. At the beginning of phase 4, the Instruction Counter is placed in PSAR #2 and the data registers are stored.

Two-Cycle Instructions

Some instructions require more than two Process Storage cycles for execution. Phases 1 and 2 of these instructions are the same as those for one-cycle instructions and are explained in Section 4.2. Phases 3 through 6 depend on the specific instruction.

Indirect and Branch Indirect Instructions (Except Storage-to-Storage Instructions)

During phase 3 of an indirect type instruction (Figure 9), the Address in the PSDR is placed into the Process Storage Address Register 2. During phase 4, the Address is incremented, if specified in the instruction, and the content of the PSDR is read back into Process Storage. Just prior to phase 5, Process Storage is read using the indirect address. During phase 5, the instruction is executed. Phase 5 of an indirect instruction is similar to phase 3 of a non-indirect instruction. During phase 6, the Instruction Counter is placed in PSAR #2, the data registers are stored and PSAR #2 is shifted to address the next instruction.

Storage-to-Storage Instructions

Phase 3 of a Storage-to-Storage Instruction is idle (Figure 10). The Instruction Counter is placed in PSAR #2 during phase 4, since it will not be available from the CSDR for use during phase 6. If the instruction is indirect, the Address of the Process Storage Data Register is placed in PSAR #1 at the end of phase 4. Since Process Storage has been written at this time, it is too late to increment the Address. Therefore, there can be no indirect and increment Storage-to-Storage Instruetions. The appropriate* Control Storage Word is read out for the second Process Cycle prior to phase 5. During phase 5, the address or word specified by the instruction is moved from

*In modes other than Channel Service, the word is addressed by the 7-bit R and S field of the instruction. In Channel Service Mode, it is the word addressed by the Channel Service Register.

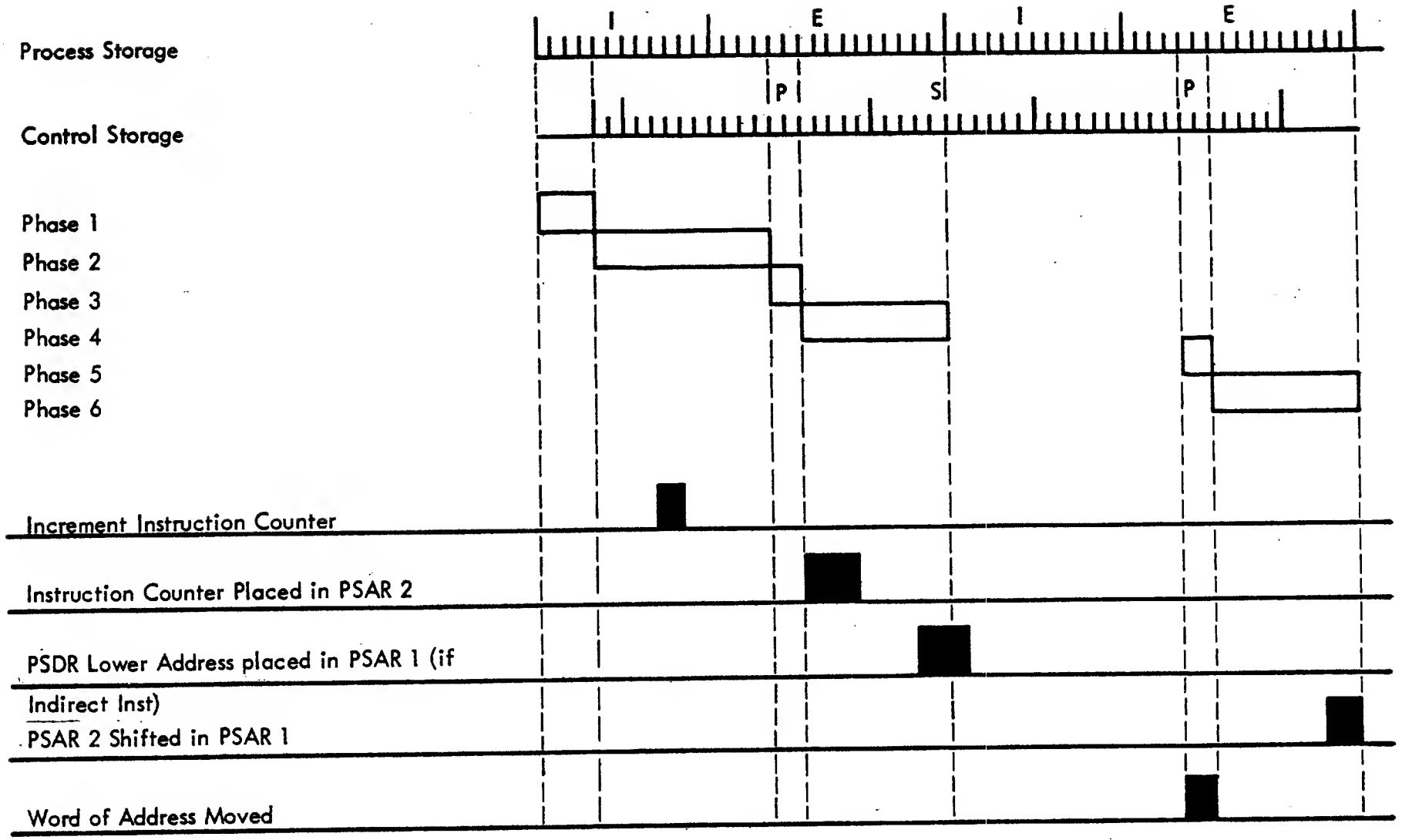


FIGURE 10 STORAGE INSTRUCTIONS

one storage to another. During phase 6, the data registers are stored. The Instruction Counter in PSAR #2 (placed there during phase 4) is put into PSAR #1 to address the next instruction.

INSTRUCTIONS

All 7750 instructions belong to one of four types:

1. Character Manipulating Instructions - CH
2. Address and Limit Moving Instructions - AL
3. Storage-to-Storage Data Transfer Instructions - SS
4. Control Instructions - CT

Addressing

The IBM 7750 is a single address machine. Each instruction contains one address for addressing storage. However, the addressing format of this machine includes address modification and indirect addressing.

Instruction Word Address - W

All 7750 instructions contain a 16-bit address (W) in bit positions 47 to 32. For direct, unmodified Character Manipulating Instructions, W is the location in Process Storage of one of the characters to be manipulated. In the execution of the other three types of direct, unmodified instructions, the 14 high order bits (47-34) address the word to be used in the execution of the instruction. The 2 low order bits of the 16-bit address are not used because these instructions deal with words in storage rather than characters. With Character Moving Instructions, however, both the word and the specific character (0, 1, 2, or 3) within the word must be specified. Therefore the complete 16-bit address must be used.

Address Modification

With the exception of all branch instructions other than Branch Indirect, the Address W of any instruction may be modified by specifying a non-zero value for the L field of the Instruction Word. If L is zero, no modification takes place. If L is non-zero, the M field (bits 20-18) specifies the register containing the modifier and L is a binary number specifying the number of bits of the modifier to be used, counting from the low order end of the specified register. L cannot be larger than eleven. The effective Address W_e is formed in the PSAR #1 by replacing the low order L bits of W by the low order L bits of the modifier in the register specified by M. The Address W is read back into storage as W rather than W_e because the read-back process was done before address modification. Table B-1 lists the value of M and the register each value specifies.

Indirect Addressing

In executing directly addressed instructions, W_e is the location of one of the operands. When an execution is executed indirectly, the operand is located at W*, and W* is the Address (bits 47 through 32) contained in the word addressed by W_e.

Register Addressing - R, S, and OAR

All Character Manipulating Instructions deal with two character locations, one in Process Storage specified by W_e or W* and the other a register specified by R (bits 29-27). S (bits 26-23) is a binary number specifying the size of the character to be operated on, counting from the low order bit of the register specified by R. In Character Manipulating Instructions, S cannot be larger than eleven. Table B-1 lists the values of R and the registers each value specifies.

Address and Limit Moving Instructions must specify the 16 bit Operational Address Register as one of their operands because the other registers are too small to accommodate the Address or Limit. The OAR is composed of the Y register and 5 low order bits of the X register. When an address or limit is moved into the OAR, the 5 low order bits of the address or limit go to the 5 low order bit positions of the X register and the 11 high order bits of the address or limit go to the Y register.

Control Storage Addressing

Storage-to-Storage Instructions deal with two word locations: one in Process Storage, specified by W_e or W*, and one in Control Storage, specified by R and S in all Modes except Channel Service. In Channel Service Mode, Storage-to-Storage instructions are executed using the contents of the Channel Service Register to address Control Storage.

TABLE B-1 - ADDRESSABLE REGISTERS

R	M	Registers
000	000	No register
001	001	X
010	010	Y
011	011	Z
100	100	Channel Service
101	101	Interface Data
110	110	Interface Control
111	111	Mode Request

Address Incrementing

If the last alphabetic code character of an operation code mnemonic is an I, W* will be incremented after its use. Address incrementing may occur whether or not W* is used as an indirect address. Incrementing starts with bit 32 of the word addressed by W_e (bit 1 of W*).

Indirect Addressing With Incrementing - Skip

All 7750 instructions whose mnemonic codes end in I* are skip instructions. If, after incrementing, bits 5-1 of W* are all Ones, the IBM 7750 executes the next instruction in sequence. Ones in bit positions 5-1 mean that the 7750 has reached the last character position of a block. To proceed any further, the 7750 must locate a new block of characters when it is receiving data or a new empty block when it is transmitting data. Therefore the next instruction in sequence is a Branch instruction which enables the 7750 to enter the subroutine for locating the next block of characters to be sent out or the next empty block to be filled.

If bits 5-1 of W* are not all Ones after incrementing, indicating that the last (32nd) character position of the block has not been reached, the 7750 skips the Branch instruction and executes the instruction following.

Flags

Bits 12 and 13 of an Instruction Word are Flag bits. Any combination of these two Flag bits may be used in an instruction. If bits 12 is a One, the Z register is decremented by one between the address modification and execution times of the instruction. If bit 13 is a One, no mode change can take place between the execution of the instruction containing this Flag bit and the next instruction executed.

Operation Code

Bit 10 through 1 of the Instruction Word is the Operation Code. It specifies what instruction the 7750 is to do. Bit 11 is the odd parity bit for bits 10 through 1 and the Flat bits.

DESCRIPTION OF INSTRUCTIONS

The instruction descriptions are arranged as follows in the text:

Instruction Name:		Load Character Indirect	
Example:		2 LOD* W 1312	
2	LOD*	W	1302
Execution length in cycles (28	Mnemonic Op Code *Indirect Address	Direct Unmodified or Modified Address	Octal Op Code, Not Incl. Parity or Flags

NOTE: Unless stated otherwise, all instructions may be executed using W_e = W modified by M and L. In all cases where modification is allowed, any of the registers in Table B-1, including no register, may be used.

Character Operations

None of the instructions in this group may be used to alter bits 1 through 7 of the Channel Service Register. Specifying R = 4 on a Load Instruction will reset the error indicators (CSR 8-11), but will not change the test of the CSR. All instructions whose mnemonic begins with X must specify R = 1, the X Register. None of the instructions whose mnemonic begins with A can specify R = 5, the Interface Data Register.

Load Character

1 LOD W 1302

All bits of register R are cleared and the lower S bits are replaced by the corresponding bits of the character addressed by W_e. The contents of storage are unchanged.

Load Character Indirect

2 LOD* W 1312

Same as LOD with indirect addressing.

Load Character and Increment

1 LOI W 1322

Same as LOD with increment.

Load Character Indirect and Increment

2 LOI* W 1332

Same as LOD with indirect and increment.

Load Complemented Character

1 LDC W 1342

All bits of register R are cleared and the lower S bits are replaced by the One's complement of the corresponding bits of the character addressed by W_e. The contents of storage are unchanged.

Load Complemented Character Indirect

2 LDC* W 1352

Same as LDC with indirect addressing.

Load Complemented Character and Increment

1 LCI W 1362

Same as LDC with increment.

Load Complemented Character Indirect and Increment

2 LCI* W 1372

Same as LDC with indirect and increment.

Unload Character

1 UNL W 1202

All 11 bits of the character addressed by W_e are cleared and the S low order bits are replaced by the corresponding bits of register R. The contents of R are unchanged.

Unload Character Indirect

2 UNL* W 1212

Same as UNL with indirect addressing.

Unload Character Indirect and Increment

2 ULI* W 1232

Same as UNL with indirect addressing and increment.

Unload Complemented Character

1 ULC W 1242

All 11 bits of the character addressed by W_e are cleared and the lower S bits are replaced by the One's complement of the corresponding bits of register R. The contents of R are unchanged.

Unload Complemented Character Indirect

2 ULC* W 1252

Same as ULC with indirect addressing.

Unload Complemented Character Indirect and Increment

2 UCI* W 1272

Same as ULC with indirect addressing and increment.

Exclusive OR

1 X OR W 1101

The S low order bits of register X are EXCLUSIVE - OR'ed, bit by bit, with the corresponding bits of the character addressed by W_e. The results replace the S low order bits of X. The contents of storage and the 11 minus S high order bits of X are unchanged. The result of an EXCLUSIVE - OR between two bits is a One when the two bits differ (10 or 01) and a Zero when they are the same (11 or 00).

Exclusive OR Indirect

2 X OR* W 1111

Same as X OR with indirect addressing.

Exclusive OR and Increment

1 XOI W 1121

Same as XOR with increment.

Exclusive OR Indirect and Increment

2 XOI* W 1131

Same as XOR with indirect addressing and increment.

Exclusive OR Complemented

1 XOC W 1141

The S low order bits of register X are EXCLUSIVE - OR'ed, bit by bit, with the One's complement of the corresponding bits of the character addressed by W_e. The results replace the S low order bits of X. The contents of storage and 11 minus S high order bits of X are unchanged.

Exclusive OR Complemented Indirect

2 XOC* W 1151

Same as XOC with indirect addressing.

Exclusive OR Complemented and Increment

1 XCI W 1161

Same as XOC with increment.

Exclusive OR Complemented Indirect and Increment

2 XCI* W 1171

Same as XOC with indirect addressing and increment.

Inclusive OR

1 IOR W 1102

The S low order bits of register R are OR'ed bit by bit with the corresponding bits of the character addressed by W_e. The results replace the S low order bits of R. The contents of storage and the 11 minus S high order bits of R are unchanged. The results of an OR between two bits is a One when either or both of the bits are Ones (11, 10, 01) and a Zero when they are both Zeros (00).

Inclusive OR Indirect

2 IOR* W 1112

Same as IOR with indirect addressing.

Inclusive OR and Increment

1 IOI W 1122

Same as IOR with increment.

Inclusive OR Indirect and Increment

2 IOI* W 1132

Same as IOR with indirect addressing and increment.

Inclusive OR Complemented

1 IOC W 1142

The S low order bits of register R are OR'ed, bit bi bit, with the One's complement of the corresponding bits of the character addressed by W_e. The results replace the S low order bits of R. The contents of storage and the 11 minus S high order bits of R are unchanged.

Inclusive OR Complemented Indirect

2 IOC* W 1152

Same as IOC with indirect addressing.

Inclusive OR Complemented and Increment

1 ICI W 1162

Same as IOC with increment.

Inclusive OR Complemented Indirect and Increment

2 ICI* W 1172

Same as IOC with indirect addressing and increment.

OR to Process Storage

1 ORP W 1002

The S low order bits of the register R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W_e. The results replace the S low order bits of the character in storage. The contents of R and the 11 minus S high order bits of the character in storage are unchanged.

OR to Process Storage Indirect

2 ORP* W 1012

Same as ORP with indirect addressing.

OR to Process Storage Indirect and Increment

2 ORI* W 1032

Same as ORP with indirect addressing and increment.

OR Complement to Process Storage

1 OCP W 1042

The One's complements of the S low order bits of the register R are OR'ed, bit by bit, with the corresponding bits of the character addressed by W_e. The results replace the S low order bits of the character in storage. The contents of R and the 11 minus S high order bits of the character in storage are unchanged.

OR Complement to Process Storage Indirect

2 OCP* W 1052

Same as OCP with indirect addressing.

OR Complement to Process Storage Indirect and Increment

2 OCI* W 1072

Same as OCP with indirect addressing and increment.

AND

1 AND W 1145

The S low order bits of the register R and AND'ed bit by bit with the corresponding bits of the character addressed by W_e. The results replace the S low order bits of R. The contents of storage and the 11 minus S high order bits of R are unchanged. The result of an AND between two bits is a One when both bits are One's (11) and a Zero otherwise (10, 01, 00).

AND Indirect

2 AND* W 1155

Same as AND with indirect addressing.

AND and Increment

1 ANI W 1165

Same as AND with increment.

AND Indirect and Increment

2 ANI* W 1175

Same as AND with indirect addressing and increment.

AND Complemented

1 ANC W 1105

The S low order bits of register R are AND'ed, bit by bit, with the One's complement of the corresponding bits of the character addressed by W_e. The results replace the S low order bits of R. The contents of storage and the 11 minus S high order bits of R are unchanged.

AND Complemented Indirect

2 ANC* W 1115

Same as AND with indirect addressing.

AND Complemented and Increment

1 ACI W 1125

Same as ANC with increment.

AND Complemented Indirect and Increment

2 ACI* W 1135

Same as ANC with indirect.

Address and Limit Moving Operations

Get Address

1 GTA W 0702

The Operational Address Register (OAR) is cleared, then loaded with the Address in the word addressed by W_e. The contents of storage are unchanged as are the 2 high order bits (10 and 11) of register S. Bits 9-6 of the X register are cleared.

Get Address Indirect

2 GTA* W 0712

Same as GTA with indirect addressing.

Get Limit

1 GTL W 0302

The OAR is cleared, then loaded with the Limit in the word addressed by W_e. The contents of storage are unchanged, as are the 2 high order bits of register X. Bits 9-6 of the X register are cleared.

Get Limit Indirect

2 GTL* W 0312

Same as GTL with indirect addressing.

Get and OR Address

1 GOA W 0502

The contents of the OAR is inclusive OR'ed into the OAR with the corresponding bits of the Address in the word addressed by W_e. The word in the Process Storage Location addressed by W_e is unchanged.

Get and OR Address Indirect

2 GOA* W 0512

Same as GOA with indirect addressing.

Get and OR Limit

1 GOL 0102

The contents of the OAR is inclusive OR'ed into the OAR with the corresponding bits of the Limit in the word addressed by W_e. The word in the Process Storage location addressed by W_e is unchanged.

Get and OR Limit Indirect

2 GOL* W 0112

Same as GOL with indirect addressing.

Put Address

1 PTA W 0602

The Address field (bits 47 through 32) in the word addressed by W_e is cleared, then loaded with the contents of the OAR. The OAR is unchanged.

Put Address Indirect

2 PTA* W 0612

Same as PTA with indirect addressing.

Put Limit

1 PTL W 0202

The Limit field (bits 27 through 12) in the word addressed by W_e is cleared, then loaded with the contents of the OAR. The OAR is unchanged.

Put Limit Indirect

2 PTL* W 0212

Same as PTL with indirect addressing.

Storage-to-Storage Data Moving Operations

See paragraph on Control Storage Addressing.

Transmit Address to Process Storage

2 TAP W 0606

The Address field in the word addressed by W_e is cleared, then loaded with the Address from the Control Storage word referenced. Control Storage is unchanged.

Transmit Address to Process Storage Indirect

2 TAP* W 0616

Same as TAP with indirect addressing.

Transmit Address to Control Storage

2 TAC W 0706

The Address field (bits 47 through 32) of the Control Storage word referenced is cleared, then loaded with the Address in the word addressed by W_e. Process Storage is unchanged.

Transmit Address to Control Storage Indirect

2 TAC* W 0716

Same as TAC with indirect addressing.

Transmit and OR Address to Control Storage

2 TOC W 0506

The Address field (bits 47-32) of the Control Storage Word referenced in inclusive OR'ed into itself with the Address field of the word addressed by W_e. The word in Process Storage location addressed by W_e is unchanged.

Transmit and OR Address to Control Storage Indirect

2 TOC* W 0516

Same as TOC with indirect addressing.

Move Word to Process Storage

2 MWP W 0206

The word addressed by W_e is replaced by the Control Storage word referenced. Control Storage is unchanged.

Move Word to Process Storage Indirect

2 MWP* W 0216

Same as MWP with indirect addressing.

Move Word to Control Storage

2 MWC W 0306

The Control Storage word referenced is replaced by the Process Storage word addressed by W_e. Process Storage is unchanged.

Move Word to Control Storage Indirect

2 MCW* W 0316

Same as MWC with indirect addressing.

Move Word and OR to Control Storage

2 MOC W 0106

The contents of the Control Storage word referenced is inclusive OR'ed into the Control Storage word referenced with the contents of the Process Storage word addressed by W_e. The word at the Process Storage location addressed by W_e is unchanged.

Move Word and OR to Control Storage Indirect

2 MOC* W 0116

Same as MOC with indirect addressing.

Control Operations

Branch type instructions other than Branch Indirect cannot have their addresses modified by M and L.

Branch

1 BRA W 0707

This instruction causes the 7750 to take its next instruction from word location W and to proceed from there.

Branch Indirect

1 BRA* W 0717

This instruction causes the IBM 7750 to take its next instruction from word location W* and to proceed from there. W* is the Address at word location W_e = W modified by M, L. See paragraph on Indirect Addressing.

Branch on Zero

1 BRZ W 0704

If the S low order bits of register R are all Zero, the 7750 takes its next instruction from word location W and preceeds from there. Otherwise, it takes the next instruction in sequence. R is unchanged.

Branch on Zero Indirect

1 BRZ* W 0714

See BRA* and BRZ.

Branch on Ones

1 BRO W 0744

If the S low order bits of register R are all One, the 7750 takes its next instruction from word location W and proceeds from there. Otherwise, it takes the next instruction in sequence. R is unchanged.

Branch on Ones Indirect

2 BRO* W 0754

See BRA* and BRO.

Branch on Test

1 BRT 0544

The contents of positions 33 through 23 of the Instruction Word are inclusive OR'ed with the contents of the register specified by the M field of the Instruction Word. If the result is all Ones, the next instruction will be taken from the location specified in the Address field (bits 47-34) of the BRT Instruction Word. If the result is not all Ones, the 7750 executes the next instruction in sequence. The contents of the Instruction Word and of the register specified by M are unchanged.

Compare Address to Limit

1 CAL W 0003

If the Address and Limit fields of the word addressed by W_e are identical, the 7750 takes the next instruction in sequence. If they are not identical, the 7750 skips the next instruction and proceeds from there. Storage is unchanged.

Compare Address to Limit and Increment

1 CAI W 0023

Same as CAL with increment.

Sense

1 SNS W 0000

The sense line as specified by the M field, $(1 \text{ to } 5)_8$, is raised for 20 microseconds. This instruction is used for diagnostic purposes only.

PRIORITY PROCESSING

When the IBM 7750 is executing a program, the sequence of its operation is controlled by the Instruction Counter. Since the Instruction Counter is not an actual register but is a field stored in a Control Storage Process Word, a change in the sequence of operation can be accomplished by accessing a different Process Word, and thereby a different Instruction Counter. In the 7750, priority processing is accomplished by the use of six such Process Words. Each Process Word has a preassigned priority. The choice of a specific Process Word is based on external conditions.

The 7750 is in a particular mode when its sequence of operation is under the control of the Process Word associated with that Mode. A Mode is requested by the setting of its associated trigger in the Mode Request Register, except for the Normal Mode, which is always requested although it has no trigger. In all Modes except Copy Mode, the 7750 operates as described in Section 4. The operation in Copy Mode is described in Section on Transmission Between the 7750 and the Computer. Table 1 gives the priority, MRR position and Control Storage address of each mode.

TABLE 1

Mode	Priority	MRR	Control Storage Address
Service	1	1	37_8
Channel Service	2	2	77_8
Copy	3	3	137_8
OUT*	4	4	136_8
IN*	5	5	176_8
Normal	6	None	177_8

*The IN and OUT Modes correspond to the Write and Read operations. They refer to the data transmission relative to the IBM 7750.

Service Mode

The Service Mode has highest priority. In most cases, this mode is used for detecting environmental errors, and the request of this mode is automatic through channel words. In addition, the Service Mode, together with the Service Mode program, may be used to: (1) isolate or remove mistakes from a program (debugging); (2) locate a faulty

component (diagnosing); and (3) obtain a programmed output of error messages when a machine malfunction occurs. Service mode may be entered manually from the operator's panel, automatically on the occurrence of an error condition, or by program. The 7750 program must enable the machine to leave this mode.

Channel Service Mode

Channel Service Mode has second priority. This mode causes the execution of the program that assigns blocks to receiving and transmitting communication channels. Channel Service Request is set automatically when any communication channels need it, and turned off by the program.

Copy Mode

Copy Mode has third priority and is requested by the program of some other mode. When this mode is operative, data are automatically moved to or from the associated computer. Copy mode is not a program executing mode but is given a mode position because its function ranks in priority above all but Service Mode and Channel Service Mode.

Out Mode

Out Mode has fourth priority. Its mode program executes the necessary instructions to set up the Copy Mode process word and prepares the 7750 to transmit data to the computer. The Out mode request bit is normally turned on by the program of the associated computer and is turned off by the IBM 7750 program. This mode may also be requested by the 7750 program.

In Mode

In Mode has fifth priority. It is requested by action of the associated computer when the computer wants the 7750 to accept data from it. The program written for this mode locates space for the data, sets up copy mode process word to read the data into this area, and requests copy mode. The In mode request bit is normally turned on by the program of the associated computer and is turned off by the IBM 7750 program.

Normal Mode

Normal Mode has lowest priority. It causes the execution of the normal program which performs error checking, code translation, recognition of functional codes, monitoring, queuing, and so on. All 7750 functions not specifically delegated to other modes usually are executed by the Normal Mode program.

Mode Selector System

The Mode Selector System enables the 7750 to change modes automatically. This system consists of a mode request register and a mode status register. Both registers have five bit positions. Each bit position in the registers represents a specific mode. Normal mode is indicated when there are no bits appearing in either register. If more than one bits appear in the MRR, indicating more than one modes are requested at the same time, only the bit corresponding to the highest requested mode appears in the MSR. Since during the Process cycle, the Control Storage is addressed by the Mode Status Register, the 7750 will always service the mode with the highest priority first.

At the end of the last Execute cycle of each instruction, the MSR is checked against the MRR. If the check shows the MSR to be at the highest requested mode, the next instruction, whose address was supplied by the previous Process cycle of the current mode, is executed. If the check shows that the MSR is not at the highest requested mode, and the instruction executed was not flagged Prevent Mode Change, the following sequence of events occurs. The MSR is updated to agree with the highest priority in the MRR; the Mode Change Trigger is set to store the fact that a mode change is to occur; the following Instruction and Execute Cycles are not used for a fetch and execute; instead, the updated MSR addresses the Process Word of the new mode in Control Storage; the Instruction Counter is used to address Process Storage on the second Instruction Cycle. The Mode has now changed with a loss of one machine cycle.

If the instruction just executed had been flagged Prevent Mode Change, the change in the MSR and the setting of the Mode Change Trigger would not have occurred. The change of mode would not have taken place until after the execution of an instruction not flagged Prevent Mode Change.

Note the following:

(1) A Character Interrupt occurring at the same time as a mode change merely causes the mode change to be delayed.

(2) A mode change cannot occur between the first and second cycles of a two cycle instruction.

CHANNEL INPUT/OUTPUT

In the 7750, the sending and receiving of data is an automatic function controlled by a unique Channel Word located in the Control Storage for each communication channel. This receiving and sending of data requires only an occasional supervision from the program.

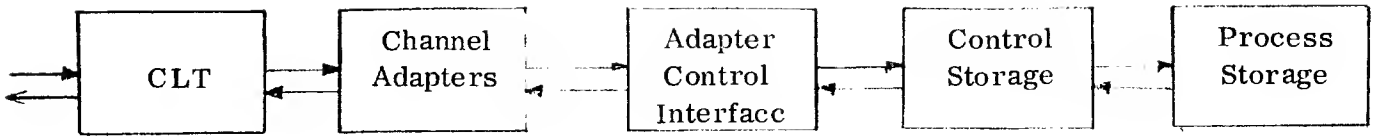


FIGURE 11 - DATA FLOW

Rcferring to Figure 11, incoming data arrive at the adapters where the data are converted (voltage levels, polarity, etc.) and sent to the Control Storage via the Adapter Control Interface. Incoming bits are maintained in Control Storage until a complete character is reccived. Then, the character is automatically transferred to Process Storage. Outgoing data are sent to the adapters serial by bit from Control Storage until a complete character has been transmitted. Then the next character is automatically obtained from Process Storage.

Adapter Control Interface

Figure 12 shows the lines which go between each of the Process Control channels and the associated adapters. Each one of these lines performs specific functions for controlling data flow between a Process Control channel and its associated adapter. Collectively, these lines form an interface -- the Adapter Control Interface.

Process Control Channel Scanner Operation

The Process Control Channel Scanner steps from channel to channel in sequence. It selects a Process Control channel every 28 microseconds (one machine cycle). The 7750 can have a maximum of 16 Process Control Channels. Depending on the application, the Process Control Channel Scanner is pre-set using a pluggable block, to count up to the maximum number of Process Control Channels used.

Channel Word

The Channel Word, a 48 bit word located in Control Storage, which automatically controls the assembly and distribution of characters to and from the channel adapters. Each communication channel connected to the 7750 has a unique Channel Word associated with it stored in Control Storage. At the beginning of each Scan cycle, the Process Control Channel Scanner selects a channel adapter. The corresponding adapter then provides the address of the correct Channel Word to the Process Control. Depending on the contents of this Channel Word, automatic character assembly and distribution takes place. The Channel Word is then stored and the Process Control Channel Scanner incremented to select the next adapter for the following Scan cycle. If in a particular application, there are ten Scan Points, Scan Point one would be selected every 280 microseconds (ten machine cycles).

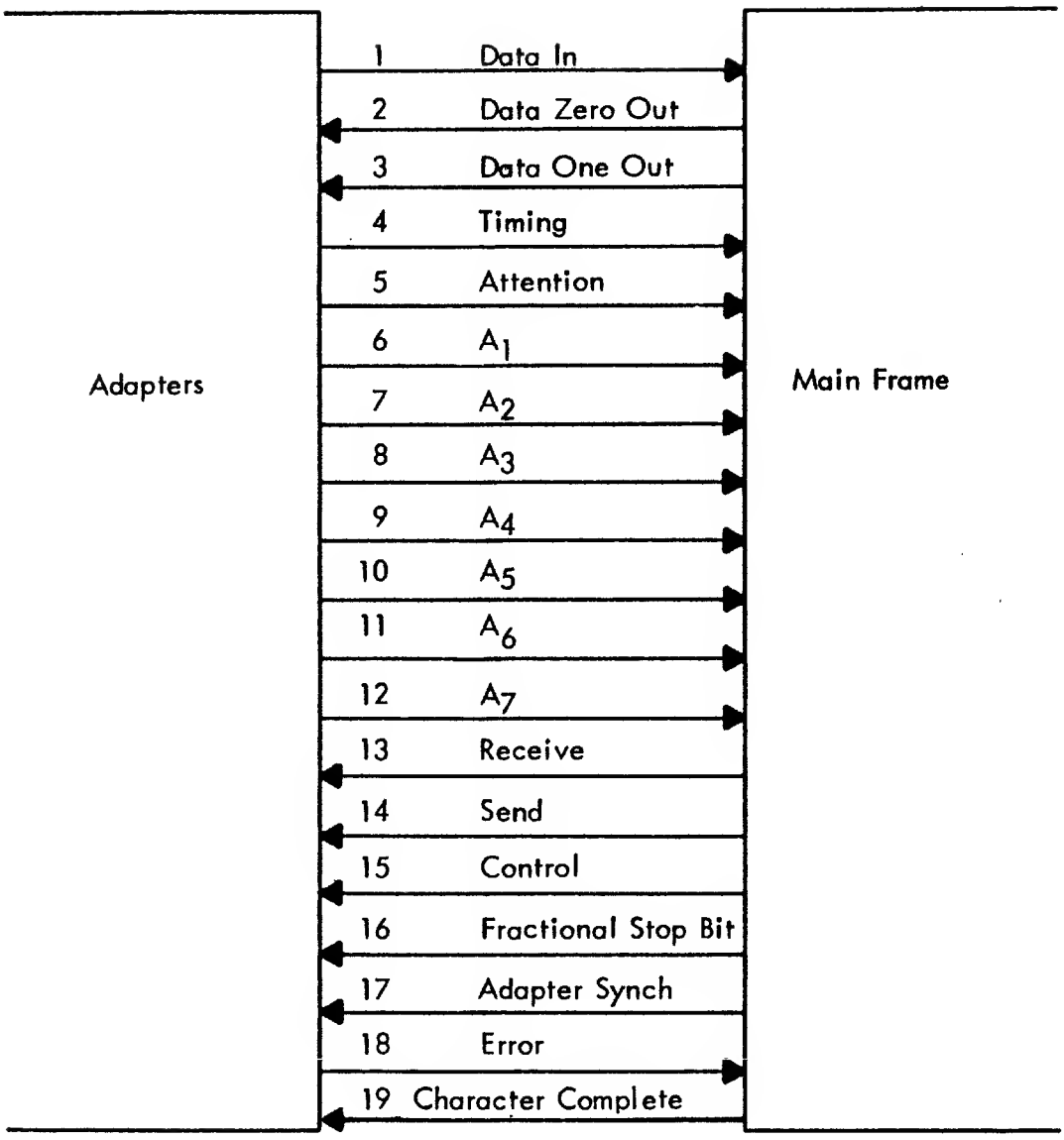


FIGURE 12 ADAPTER CONTROL INTERFACE

Channel Word Format

The Channel Word is composed of the following fields (Table 2).

TABLE 2 - CHANNEL WORD FORMAT

Position No.	Name	Field
47-34	Word Address	W
33-32	Character	A
31	Last Timing	B
30-27	Character Length	C
26-23	Status-Micro	D
22-20	Action	E
19-15	Character Control	F
14-12	Status-Macro	G
11-1	Assembly/Distribution	H
P	Word Parity	---

The Assembly/Distribution field, H, is an eleven bit shift register and count-down counter which contains all or a portion of a character being assembled or distributed. Characters are arranged in the H field with the first bit placed in the low-order position. The character length field, C, defines the number of bits per character. Fractional Stop bits are omitted when determining the character length.

Since in each Process Storage word, four characters can be stored, the Character field, A, defines the next character position in the Process Word to be assembled or transmitted. Character field A is automatically incremented each time a new character is transferred to or obtained from storage.

The Word Address field, W, defines the Process Storage word location of the next character position. It is automatically incremented when four character positions have been used.

In the G field, the high-order bit defines the type of character transmission; Synchronous or Start-Stop. The next high-order bit CSDR 13, is defined later in this manual for Start-Stop channel words and for Synchronous channel words. The Lower Order bit indicates whether the 7750 is sending or receiving data.

The Last Timing bit, B, is used in conjunction with the Timing Line of the Adapter Control Interface. At the beginning of each Scan cycle, the Last Timing bit is EXCLUSIVE - OR'ed with the Timing Line to determine if a new bit time has occurred. A difference is interpreted as a demand by the channel adapter for the next data bit to be transmitted or received by the Process Control. Following a bit transfer, the Last Timing Bit is automatically set equal to the Timing Line.

Fields D and F are discussed in succeeding sections. Their functions depend on the type of character transmission and the status of the Channel Word. The Action field, E, is discussed in the section, Action Delaying Feature.

Character Assembly and Distribution

Characters are automatically loaded into the assembly area (H field) and send to the channel adapter, serial by bit from the low-order position, at each new bit time.

For Start-Stop or Synchronous data transmission, the four low-order bits in the Character Control Field, F, form a binary counter which increments each time a new bit is sent to the channel adapter. When the bit count equals the Character Length, signifying that a complete character has been sent to the adapter, the next character is automatically obtained from Process Storage.

In a receiving status, incoming bits are gated into the Assembly Area, as defined by the Character Length Field (C), and shifted toward the low-order bit position. For example if C equals 11_8, the first bit and all succeeding bits of the character enter at CSDR bit position 9.

For Synchronous receive the complete character is stored when the four low-order bits of F equal C. However, on Start-Stop receive, a different method is used to determine when a complete character is in the Assembly Area. The detection of the start bit shifting into the CSDR 1 and a stop bit shifting into H, as defined by the Character Length Field (C), causes the character to be stored. Before storing the character, the Assembly Area is again shifted to strip the start bit from the character. On Start-Stop receive, the F field is not used as a counter.

Data Transfer Check

An automatic Data Transfer Check is made on the data flow path between the Process Control and the channel adapter in Send Status. Each time a data bit is sent to the channel adapter, it is retained in the low-order position of the D field in the Channel Word. This low order position of the D field is the Transfer Check bit (CSDR 23). When the IBM 7750 is sending data to a communication channel, the channel adapter sets the value of the last bit sent to the communication channel on the Data-In line. When the next bit is requested by the channel adapter, the Transfer Check bit is compared with the Data-In line. If they do not compare, a Channel Error is indicated (see Section on Channel Error). The MCA also makes a check on the data flow path between the MCA data bit and the output communication lines of the Communications Line Terminator (CLT).

Start-Stop Channel Words

Channel Words would normally be assembled by the program in Process Storage and transferred to Control Storage to initiate character assembly or distribution. The Channel Word as it is used for Start-Stop channels is given in Table 3 and Figure 13. All unused bits must be logical Zeros in Start-Stop Channel Words.

Certain ground rules are necessary to insure correct data transmission. One such rule is Adapter Synchronization. If a channel has been inactive, i.e., hold status, or the data flow direction has changed, it is necessary to use the first active Scan cycle to synchronize the adapter with the Process Control. This should not be confused with Synchronous transmission. In the new Channel Word the programmer must set the Character Control field, F, to 14_8. On the first active Scan cycle the Channel Word automatically performs the following functions:

1. The Last Timing bit is reset to a logical Zero.

2. A Data Transfer Check is inhibited, and the Transfer Check bit reset to a logical Zero.

3. The Adapter Sync line is set to a logical One.

4. If the channel is starting to send, the first character of the message is obtained from Process Storage.

5. The Character Control field is reset to 00_8 for use as a bit counter.

6. CSDR bits 11-1 are cleared.

TABLE 3 - START-STOP CHANNEL WORD FORMAT

Position No.	Name	Field
47-34	Word Address	W
33-32	Character	A
31	Last Timing	B
30-27	Character Length	C
26	Not Hold	D
25	Delay	D
24	Fractional Sampling Bit	D
23	Transfer Check	D
22-20	Action	E
19-15	Character Control	F
14-12	Status-Macro	G
11-1	Assembly/Distribution	H
P	Word Parity	---

In send status, for channels having character formats containing non-integer stop bits, the programmer must set the Fractional Sampling Bit in the D field to a logical One. When Bit Count equals Character Length, signifying that the last stop bit is being sent to the adapter, the Fractional Sampling Bit line of the Adapter Control Interface

START-STOP CHANNEL WORD FORMAT

FIELD	W	A	B	C	D	E	F	G	H	P
~~CSDR Bit Post. No.~~ NO. OF BITS PER FIELD	14	2	1	4	4	3	5	3	11	1
CSDR Bit Post. No.	47-34	33-32	31	30-27	26-23	22-20	19-15	14-12	11-1	1
SEND*										
1. First Active Scan Cycle	Word Addr. of 1st Char.	Char.	0	02-13	10	0	14	3	0000	-
2. Normal Without Error	---------	----	-	02-13	10-11	0	00-13	3	----	-
3. Normal Delay Without Error	---------	----	-	02-13	14	0	00	3	----	-
RECEIVE*										
1. First Active Scan Cycle	Word Addr. of 1st Char.	Char.	0	02-13	10	0	14	2	0000	-
2. Normal Without Error	---------	----	-	02-13	10	0	00	2	----	-
3. Normal Delay Without Error	---------	----	-	02-13	14	0	00	2	----	-
INACTIVE Send or Receive	---------	----	-	----	00-07	-	----	0 or 2	----	-

*Without Fractional Stop Bit
Note: All numbers in octal

FIGURE 13

is automatically set to a logical One. The adapter will then elongate this last stop bit by a predetermined interval.

The programmer can automatically initiate a sending delay during the normal transmission of a message. The programmer inserts in the message a special character followed by a delay count equal to the desired delay in binary bit times. The special character is called Special Sending Delay Character (SSDC) and has the following bit pattern: 3777_8. During a Character Interrupt the recognition of SSDC sets the Delay bit in the D field to a logical One. Character Interrupt is initiated the next time this same Channel Word is accessed and the delay count is loaded into the H field. The maximum delay is 3775_8. Each time the Channel Word is accessed and a new bit time occurs, the H field is decremented. When the H field is decremented to all Zeros, signifying the end of sending delay, the Delay bit is turned off, and the next character is obtained from Process Storage to be transmitted in the normal manner. Neither the SSDC nor the delay count is sent to the channel, nor can either be located in the 32nd position of a Block in Process Storage.

In data transmission, it is sometimes desirable to send a message and then wait for a reply on the same line, e.g., polling on half-duplex lines. The programmer can automatically initiate a status change in the Channel Word at the end of an outgoing message for this purpose. The recognition of a special character by the logic will place the Channel Word in a receiving delay status, during which time the logic examines the Data-In line for a logical One, i.e., start bit of an incoming character. The recognition of a start bit places the Channel Word in normal Start-Stop receive for character assembly. If the delay interval times out, the Channel Word will be placed in a Hold condition. The special character is defined as the Status Change Character (SCC) and has the following bit pattern: 3776_8.

To initiate a status change, the programmer inserts the Status Change Character followed by a delay count character equal to the desired delay in binary bit time. The maximum delay count that can be used is 3775_8. During a Character Interrupt, the recognition of SCC sets the Delay bit (CSDR 25) to a logical One. Character Interrupt is again initiated the next time this same Channel Word is accessed if the Data-In line is a logical Zero. The Data-In line being a logical Zero signifies that the last character was transmitted. The delay count character is loaded into the H field, the F field is set to 14_8, and the low-order bit in the G field is set to a logical Zero, i.e., receive status. On the next active Scan cycle the octal code 14_8 performs the Adapter Synchronization function. Each time this Channel Word is accessed and a new bit time occurs, the H field is decremented. If at anytime the Data-In line becomes a logical One, i.e., the start bit of an incoming character, receiving delay is terminated; the assembly area is cleared, data is entered, and the Delay bit turned off. Should the H field be decremented to all Zeros, the Not Hold bit (CSDR 26) is reset to a logical Zero placing the Channel Word in an inactive status. Neither the SCC nor the delay count character can be located in the 32nd position of a block of Process Storage.

Synchronous Channel Words

As previously mentioned, the major difference between Start-Stop and Synchronous transmission is the character format. To establish and maintain character synchronization, synchronous channels use special synchronizing characters instead of start and stop bits. However, once character synchronization has been established, incoming characters are stored regardless of the content of the assembly area. In some applications it is also desirable to transmit synchronization characters, at pre-determined intervals, to aid the maintenance of character synchronization.

Two types of character synchronization are available. They are "Hunt" and "Continuous Hunt". The choice of which type to use, or whether a combination of the two should be used, is determined by the particular application. The Channel Word format as it is used for Synchronous channels in receive status is given in Table 4 and Figure 14.

TABLE 4

SYNCHRONOUS CHANNEL WORD FORMAT - RECEIVE STATUS

Position No.	Name	Field
47-34	Word Address	W
33-32	Character	A
31	Last Timing	B
30-27	Character Length	C
26-23	Extended Assembly Area	D
22-20	Action	E
19-15	Character Control	F
14-12	Status-Macro	G
11-1	Assembly/Distribution	H
P	Word Parity	---

Before a Channel Word can be placed in Hunt or Continuous Hunt Status, it is necessary to use the first active Scan cycle to synchronize the adapter with the Process Control. The Character Control field is used to perform this function. By setting the proper octal code in the F field, the programmer can make one of several sequences take place without further attention from the program. These sequences are:

1. Adapter Synchronization going to normal synchronous receive.

2. Adapter Synchronization going to Continuous Hunt.

SYNCHRONOUS CHANNEL WORD FORMAT

	W	A	B	C	D	E	F	G	H	P
Number of Bite per Field	14	2	1	4	4	3	5	3	11	1
CSDR Bit Post. Number	47-34	33-32	31	30-27	26-23	22-20	19-15	14-12	11-1	P
SEND*										
1. First Active Scan Cycle	Word Addr. of 1st Char.	Char.	0	01-13	02	0	14	7	0000	-
2. Normal Without Error	---------	----	-	01-13	02-03	0	00-13	7	----	-
RECEIVE*										
1. First Active Scan Cycle	Word Addr. of 1st Char.	Char	0	01-13	00	0	14	6	0000	-
2. First Active Scan Cycle Going to Continuous Hunt	Word Addr. of 1st Char.	Char.	0	01-13	00	0	34	6	----	-
3. Normal Continuous Hunt	---------	----	-	01-13	--	-	10-33	6	----	-
4. First Active Scan Cycle Going to Hunt	Word Addr. of 1st Char.	Char.	0	01-13	00	0	16	6	0000	-
5. Hunt	Word Addr. of 1st Char.	Char.	-	01-13	--	0	17	6	0000	-
6. First Active Scan Cycle Going to Hunt then Going to Continuous Hunt	Word Addr. of 1st. Char.	Char.	0	01-13	00	0	36	6	0000	-
ERROR CHANNEL WORD (Send or Receive)	---------	----	-	14-17	10-11	-	--	2-3	----	-
INACTIVE SEND or RECEIVE	---------	----	-	--	00-07	-	--	0 or 2	----	-

*Control Bit CSDR 13 Logical One

Note: All numbers in octal

FIGURE 14

3. Adapter Synchronization going to Hunt and then going to normal synchronous receive.

4. Adapter Synchronization going to Hunt and then going to Continuous Hunt.

Sequence one, "Adapter Synchronization" going to synchronous receive, operates in the following manner. The programmer inserts the octal code 14_8 in the F field. When a Channel Word containing this octal code is accessed on the first active Scan cycle, the following automatic actions take place:

1. The Last Timing bit is reset to a logical Zero.

2. The D field is cleared.

3. The Adapter Synchronization line is set to a logical One.

4. The four low-order bits in the F field are reset to 00_8 for use as a bit counter.

5. The H field is cleared.

After the Adapter Synchronization function has been completed character assembly begins. The Channel Word is in a normal synchronous receive status.

Sequence Two, "Adapter Synchronization" going to Continuous Hunt, operates in the following manner. The programmer inserts the octal code 34_8 in the F field. The high-order bit in the F field defines Continuous Hunt. On the first active Scan cycle the octal code 34_8 performs the Adapter Synchronization function as described in the previous paragraph. However, when the Adapter Synchronization is completed, the Channel Word is in a Continuous Hunt status and character assembly begins.

In Continuous Hunt, a 16-bit end-around shift register is formed using bits 11-1, 26-23, and the Data-In line. A new bit is entered into the Assembly Area, as specified by C, and shifted toward the low-order position. The low-order position is equal to the Character Length plus one. If C equals 6 the low-order position is Control Storage Data Register 7. A maximum of fifteen bits are maintained in the shift register. As each new bit is received, the Bit Count is incremented and compared with the Character Length. If a comparison occurs, Character Interrupt is initiated, and those low-order bits in H as specified by the Character Length are transferred to Process Storage.

In Continuous Hunt, the 7750 examines the contents of the 16-bit Assembly Area at each new bit time. Character synchronization is established when the logic indicates that the proper synchronization pattern has been received. The four low-order bits of F are reset to 00_8 in preparation to count succeeding bits. However, the Continuous Hunt bit is not turned off. When Bit Count equals Character Length, those bits as specified by C are transferred to Process Storage. Only one synchronization pattern per Process Control Channel can be used. The selection of the correct decoder is made by the Process Control Channel Scanner.

Note that there may be some dangers inherent in the use of Continuous Hunt. Bit synchronization data may be transferred to Process Storage as if they were valid characters.

Sequence Three, "Adapter Synchronization" going to Hunt status and then going to synchronous receive, operates in the following manner. The programmer inserts the octal code, 16_8, in the Character Control field. When a Channel Word containing the octal code 16_8 is accessed on the first active Scan cycle, the following action is initiated:

1. The Last Timing bit is reset to a logical Zero.

2. The D field is cleared.

3. The Adapter Synchronization line is set to a logical One.

4. The four low-order bits of the F field are incremented to 17_8.

5. CSDR bits 11-1 and 26-23 are cleared.

After the "Adapter Synchronization" function has been completed, the octal code, 17_8, places the Channel Word in Hunt status.

In Hunt, a 16-bit end-around shift register is formed using bits 11-1, 26-23, and the Data-In line. A new bit is entered into the Assembly Area, as specified by C, and shifted toward the low-order position. The low-order position of the 16 bit Assembly Area is equal to C plus one. For example, if C equals seven, the low-order position is Control Storage Data Register 8. A maximum of 15 bits are maintained in the shift register. As each new bit is entered, the F is not incremented and characters are not transferred to Process Storage.

In Hunt, 7750 examines the contents of the 16-bit Assembly Area at each new bit time. Character synchronization is established and Hunt status is terminated when the logic indicates that the proper synchronization pattern has been received. The four low-order bits of the F field are incremented to 00_8 for use as a bit counter, and the Channel Word is in a normal synchronous receive status.

Logic is provided for two synchronization patterns. These patterns may be any combination of logical One's and Zero's and have maximum lengths of 16 bits. Only one synchronization pattern per Process Control Channel can be used. The selection of the correct decoder is made by the Process Control Channel Scanner. Hunt and Continuous Hunt must use the same synchronization pattern.

Sequence Four, "Adapter Synchronization" going to Hunt and then going to Continuous Hunt, operates in the following manner: To initiate sequence four, the programmer inserts the octal code 36_8 in the F field. Sequence three is performed, followed by sequence two. However, a second Adapter Synchronization does not occur.

It sometimes is desirable to automatically place the Channel Word in a Receiving Hunt status at the end of an outgoing message. The programmer can change the Channel Word by placing a special character at the end of the message. This special character is called Status Change Character (SCC), as described in Start-Stop Channel Words section and has the following bit pattern: 3776_8. During a Scan Cycle the recognition of SCC automatically sets the four low-order bits of the F field to 16_8 and low-order bit in the G field to a logical Zero, i.e., receiving status, if the Data-In line is a logical Zero and a timing change has occurred. The Data-In line being a logical Zero with a Timing Change signifies that the last character has been transmitted. Depending upon the high-order bit of the F field (Continuous Hunt), sequence three or four as previously described is initiated.

Table 5 gives the Synchronous Channel Word Format -- Send Status.

TABLE 5

Position No.	Name	Field
47-34	Word Address	W
33-32	Character	A
31	Last Timing	B
30-27	Character Length	C
26-25	Not Used	D*
24	Not Error	D
23	Data Transfer Check	D
22-20	Action	E
19-15	Character Control	F
14-12	Status-Macro	G
11-1	Assembly/Distribution	H
P	Word Parity	---

*All unused bits must be logical Zeros in Synchronous Send Channel Words.

If a communication channel has been inactive, i.e., hold status, or the direction of data flow has changed from receive to send, it is necessary to use the first active Scan cycle to synchronize the adapter with the Process Control. In the new send Channel Word, the programmer must set the Character Control Field, F, to 14_8 or 34_8. On the first active Scan cycle, the Channel Word automatically performs the following functions:

1. The Last Timing bit is reset to a logical Zero.

2. A Data Transfer Check is inhibited, and the Transfer Check bit reset to a logical Zero.

3. The Adapter Synchronization line is set to a logical One.

4. CSDR bits 11-1, 26-25 and 23 are cleared.

5. CSDR bit 24 is set to a logical One (not error).

6. The first character of the message is obtained from Process Storage.

7. The Character Control field is reset to 00_8 or 20_8 for use as a bit counter.

Channel Errors

A Channel Error is defined as an error that was detected by the 7750 which occurred between the Process Control character assembly/distribution area and a remote terminal. The detection of a channel error is automatic but the indication of the error as to its identity, where it occurred, and the corrective action to be taken is the responsibility of the program.

The present components attached to or contained in the 7750 may produce three different types of channel errors on high speed and two different types of channel errors on low speed communication channels.

Low Speed Channel Errors

A. Data Transfer Error

The detection of this error is based on the same principles described in the Data Transfer Check Section. The Data Transfer Error can only be detected on channels in sending status.

B. MCA Parity Error

This type of error can be detected on all low speed channels, regardless of their status. The Multiplexing Channel Adapter has a storage with 32 Control words, sub-divided into 4 eleven-bit Control characters. Each Control character in the Storage is checked for odd parity. If on a matched Scan cycle (i.e., when the MCA Control character that is read out contains information for the same channel whose CWD is located in the CSDR at the same time), the MCA detects a parity error; this error is indicated to the Process Control via the Adapter Control Interface Error line.

C. Indication of Low Speed Channel Errors to Program

Control Storage Data Register bit position 13 is used to tag the Start/Stop Channel Word when an error occurs. Bit position 13 is called the Not Error bit, i.e., CSDR 13 a logical Zero indicates an error condition. When a channel error occurs,

the Not Error bit is automatically set to a logical Zero. If the Start/Stop Channel Word is active (Not Hold status), the address of the Channel Word is placed in the Channel Service Register, Service Mode is requested, the Channel Error trigger (CSR8) is set to a logical One, and the Channel Check trigger on the operator's panel turned on, provided that:

1. CSDR 13 is a logical Zero - indicating an error.

2. Channel Service Mode has not previously been requested.

3. Service Mode has not previously been requested.

High Speed Channel Errors

Control Storage Data Register bit position 24 is used to tag the Synchronous Channel Word when a Data Transfer Check occurs. Bit position 24 is called the Not Error bit, i.e., a logical Zero in CSDR 24 indicates an error condition. The detection of this error is based on the same principles described in the Data Transfer Check Section. When a Data Transfer Check occurs, the Not Error bit (CSDR 24) is automatically set to a logical Zero, the address of the Channel Word is placed in the Channel Service Register, Service Mode is requested, the Channel Error trigger is set to a logical One, and the Channel Check trigger on the operator's panel is turned on, provided that:

1. CSDR 24 is a logical Zero.

2. Channel Service Mode has not previously been requested.

3. Service Mode has not previously been requested.

Time-Out Tag and Interlock associated with High Speed Adapter 2 for half and full duplex channels are discussed later in the HSA Section. When a high speed adapter detects one of the above errors, the adapter changes the address lines of the adapter control interface so that a CWD different from the normal CWD will be accessed the next time the adapter is selected. For each error condition a unique CWD is accessed in Control Storage. Hereafter, this new CWD will be called Error Channel Word and uses a Start/Stop CWD format with a character length field greater than 13_8 (See Table 6). The addresses in Control Storage are used to identify the type of error and the channel on which the error occurred.

When the ECWD is accessed CSDR 13 is set to a logical Zero, the address of the ECWD is placed in the Channel Service Register, Service mode is requested and the Channel Error trigger (CSR 8) turned on, provided that:

TABLE 6

ERROR CHANNEL WORDS

Position No.	Field		Logical State					
			Interlock		Carrier ON		Time-Out Tag	
			Half Duplex	Full Duplex	Half Duplex	Full Duplex	Half Duplex	Full Duplex
47-34	Word Address	W	(a)	(a)	(a)	(a)	(a)	(a)
33-32	Character	A	0	0	0	0	0	0
31	Last Timing	-	-	-	-	-	-	-
30-27	Character Length	C	(b)	(b)	(b)	(b)	(b)	(b)
26	Not Hold	D	(c)	(c)	(c)	(c)	(c)	(c)
25-23	Not Used	D	(a)	(a)	(a)	(a)	(a)	(a)
22-20	Not Used	E	(a)	(a)	(a)	(a)	(a)	(a)
19	Not Used	F	(a)	(a)	(a)	(a)	(a)	(a)
18-15	Character Control	F	(d)	(d)	(d)	(d)	(d)	(d)
14	Start Stop	G	0	0	0	0	0	0
13	Not Error	G	1	1	1	1	1	1
12	Send/Receive	G	0	0	0	0	0	0
11-1	Assembly Area	H	(a)	(a)	(a)	(a)	(a)	(a)

(a) May be used by the programmer.
(b) Must be 17_8 - 14_8
(c) Must be a logical one to activate ECWD.
(d) Used to clear error condition from adapter.

1. CSDR 26 (Not Hold) is a logical One.

2. CSDR 18-15 contains 00_8.

3. Channel Service Mode has not previously been requested.

4. Service Mode has not previously been requested.

In all cases except a Time-out Tag error, the Channel Check light on the operator's panel is turned on.

Identification of Channel Errors

Any type of channel error for high or low speed channel will automatically turn the operation of the IBM 7750 to the Service Mode. The program written for the Service Mode must have efficient routines for the quick identification of the specific error indicated and for the initiation of the corrective actions.

The program must examine the settings of the error bits (bits 11-8) in the Channel Service Register in order to execute the proper routine. Since each of the three high order bits in the CSR represents one Process Control error, and only bit 8 can indicate one of the five different types of system errors, the programmer should check bit 8 first. The next step for the programmer to do is to examine the contents of the 7 low order bit positions in the Channel Service Register, and through cross references, identify the channel being in error and the type of error. Once the error and the source is identified, the desired action can be initiated without delay.

Corrective Actions for Channel Errors

There are no set rules or methods for handling channel errors; each error condition depends entirely on the configuration and requirements of each individual system application and must be presented in the system specifications. However, certain possibilities may be pointed out on a general level. The environment of a communication network sometimes may be the source of conditions resulting in effects recognized as errors, when no error occurred. Therefore, the programmer may follow a principle of trying out the error indication first and be sure of the presence of the signal error before initiating a complicated error procedure. To do this, the programmer must eliminate the error indication by resetting Channel Words to Not Error status and keep a count for each error type, by channels at certain memory locations. If the indicated error has been a legitimate error, the Service Mode will repeatedly be requested in consecutive scan cycles for that specific channel after each resetting and the count will rapidly reach the pre-determined number required to execute certain error routine. At this time, the counter must be reset, since it is possible that the same "illegitimate" error counts.

The 7750 machine operation should be kept in the Service Mode for as short a time as possible. The 7750 should only initiate, but not execute error routines in this Mode. Executing error routines in the Service Mode would block other channels from obtaining service for this or other modes.

In the case of a Time Out Tag Error, the Service Mode Program must load the 14_8 adapter synchronization pattern into bit positions 18-15 of the affected Error Channel Word right after the identification of the error. This resets the error condition in the Channel Adapter.

If a "legitimate" error condition is found, the Service Mode Program must inactivate the channel by setting bit positions 26 and 14 of the Error Channel Word or the regular Channel Word (depending which one is used for indicating the error) to logical zeros before turning control over to the error-handling Mode. If no provision is made for this action, control will be repeatedly turned over to the Service Mode for the very same error, until the error is corrected.

If the correction of a system error requires a comparatively long time, the traffic of the affected channel most likely will be rerouted. Normally, the computer will initiate such an order. However, the system specifications and the 7750 program must have made provisions for these cases in advance.

The Service Mode Program must turn the Channel Error Bit (bit 8) in the Channel Service Register off before the Service Mode request bit is turned off in the Mode Request Register. This should be done by the instruction immediately preceeding the one that turns the Service Mode request bit off. If the instruction for turning the Channel Service Register off is given sooner, the contents of the 7 low order bit positions of the Channel Service Register may be destroyed before the Service Mode Program is able to complete the necessary identification procedure. Each time an End of Block condition is recognized in a Channel Word, the machine logic first examines the status of the Channel Error Bit in the Channel Service Register. If this bit is off (logical Zero) and the Channel Service Mode request bit is off in the Mode Request Register at the same time, the Control Storage address of the Channel Word requesting service is placed in the 7 low order bit positions of the Channel Service Register. The Channel Service Mode request bit is turned on in the Mode Request Register. This will happen, regardless whether the Service Mode request bit is on or off. Only the "on" status of the Channel Error bit prevents the machine logic from destroying the error indicating Channel Word address or Error Channel Word address in the Channel Service Register.

On the other hand, if the Service Mode Program failed to turn the Error Channel Bit off, the Channel Service Mode would be blocked for all channels until the bit is turned off. The Channel Error bit can be turned off by a (LOD) Load instruction specifying the Channel Service Register (C or 4) as an R register with blank or zero S field; this instruction resets the four high order bits (bits 11-8) in the Channel Service Register at the same time.

Action Delaying Feature

In some cases, when working with high speed lines, it is necessary to take some action relative to this line more rapidly than the normal IBM 7750 program is able to do. It also may be necessary to take this action after a delay of several character times. The sequence of recognizing a character, waiting one or more character times, and then taking some action relative to a high speed line will be called the "Action Delaying Feature". An example of its use may be found in SABRE-type systems, in which it is necessary to recognize the Go AHEAD character, wait one character time, and then raise the NEW SYNCH line to the subset.

The Action Delaying Feature enables the programmer to automatically change the E, F, and G fields of the Channel Word during character transmission. These new fields are stored in predetermined locations in Process Storage and must be loaded by the program. They are addressed by the position of the Process Control Channel Scanner, which supplies A and the two low-order bits of W. The new E, F, and G field locations for Process Control channels 1-16 are permanently wired into addresses 37774_8, 0_8 to 37777_8, 3_8, respectively.

A channel is put into the Action Delaying mode by setting the low-order bit of the E field to a logical One in the appropriate Channel Word. A count equal to 3 minus the desired number of character delays is inserted into the two high-order bits of the E field. Using a wire-in decoder, the IBM 7750 then examines in parallel the contents of the H field searching for the Action Delay character, during Character Interrupt. One Action Delay character decoder is provided for each machine.

When the Action Delay character is recognized, the low-order bit of the E field is turned off and the two high-order bits incremented. During each succeeding Character Interrupt cycle, the two high-order bits are incremented until they change to logical Zeros, signifying that the E, F, and G fields are to be changed at this time. The new fields are automatically transferred into the Channel Word during the E cycle of Character Interrupt. These fields will contain the bit pattern necessary to affect the desired change in action of this channel.

Character Interrupt

Character Interrupt is the interruption of a normal machine cycle for the purpose of transferring a received character to Process Storage or obtaining a new character from Process Storage for transmission (Figure 15). The execution of a program is not disturbed at the time Character Interrupt occurs. However, Character Interrupt does delay the program by one machine cycle. If a mode change should occur just before Character Interrupt, the Mode change is delayed by one machine cycle.

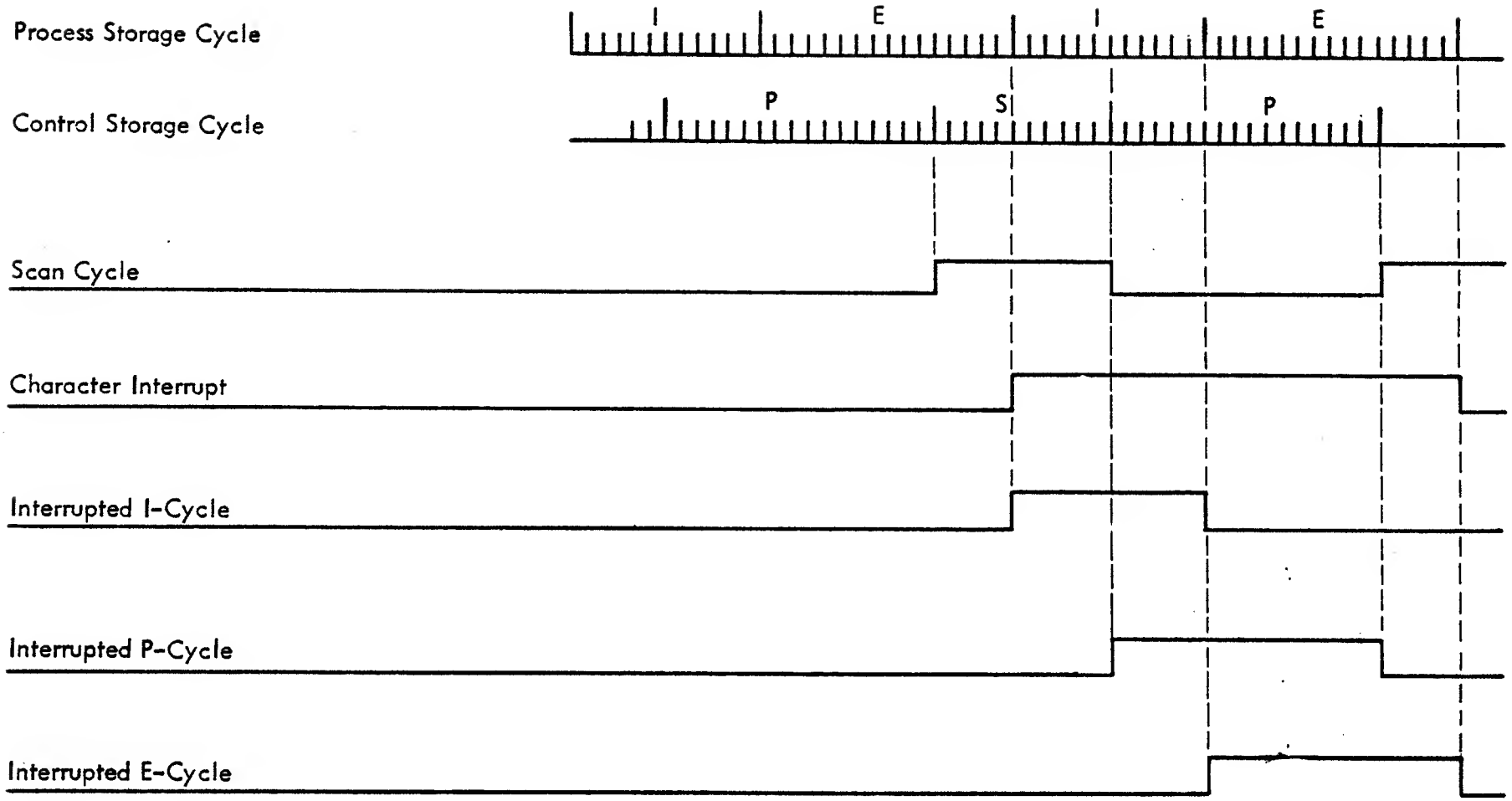


FIGURE 15 CHARACTER INTERRUPT TIMING

The Character Interrupt trigger is set when a complete character has been received or transmitted. The address of the Channel Word is held in the Control Storage Address Register during the Interrupted Process Cycle. The Address (W) in the Channel Word addresses Process Storage prior to the interrupted I cycle. During the Interrupted I cycle, the Process Storage is read, and the character is transferred via the character bus. In Start-Stop Send, Synchronous Send, and Start-Stop Receive, eleven bits are transformed to or from the character distribution of character assembly area. In Synchronous Receive, only those bits specified by the Character Length in the Channel Word are transferred to the Process Storage. At the end of the interrupted I cycle, the word in the PSDR is read back into Process Storage, and the Channel Word Address (W) is incremented. If the five low-order bits of the incremented character address are all Ones, Channel Service is requested. The Channel Word is re-stored at the end of the interrupted P cycle and Character Interrupt is terminated.

Channel Service

A Channel Service program obtains new blocks of storage for receiving channels, and locates the new next block of a sending chain for sending channels. The programmer must prepare a program for this function. The end of a block in storage is detected when the 3 low-order bits of W and the 2 low-order bits of A are all Ones. These five low-order bits request Channel Service. If the Channel Service Mode Request and Channel Error bits are off and the Channel Word does not indicate an error condition, the contents of the Control Storage Address Register are transferred to the Channel Service Register. This preserves the address of the Channel Word requiring service. The Channel Service Mode Request trigger is turned on, and a mode change occurs at the appropriate time. The Channel Service Mode Select trigger initiates the Channel Service program and the Channel Word Address is set to the starting address of a new block of storage. When Channel Service Mode is complete, the Channel Service Mode Select and Request triggers are reset.

The failure of a channel to get service before a complete character has been received will result in the loss of the character. If a complete character is transmitted before Channel Service is obtained, logical Zeros will be transmitted as the next character.

TRANSMISSION BETWEEN THE COMPUTER AND THE 7750

Two registers, the Interface Control Register (IFCR) and the Interface Data Register (IFDR), are used in conjunction with the necessary control circuits to transmit data or control information to the computer from the 7750 or to receive data control information from the computer. These two directions of transmission are the 7750 Out and In operations, respectively. The Interface Control Register is shown in Figure 6. The Interface Data Register is a one character buffer used to facilitate the character transfer.

The In Operation: Transmission from the Computer to the IBM 7750

In Mode

Transmission of data from the computer to the IBM 7750 can be initiated by the 7750 program. The program brings up the Attention line to the computer via the Attention bit in the IFCR. The computer will then bring up the Attention Response line to the 7750, which resets the Attention bit.

The computer must be programmed to bring up the Control line or Write line to the 7750. This may be done with or without a prior Attention from the 7750. The Control line will set the Control trigger of the IFCR and the In trigger of the Mode Request Register; the Write line will set only the In trigger of the Mode Request Register. This will set a Command Response trigger, the output of which is sent to the computer on the Command Response line. The 7750 will then go into the In Mode, and the program will examine the IFCR to determine whether Write or Control was given by the computer. The In Mode program will turn on the Copy trigger of the Mode Request Register (MRR), leaving the In trigger on. At the beginning of the next I cycle, Copy Mode commences. Sometime prior to entering Copy Mode, the program will have set up the Copy Word with the beginning (W) address and ending (Limit) address of the location where the data is to be stored. In this connection, it is required that the programmer establish a maximum length for messages received from the computer. This determines the Limit of the Copy Word.

During In Mode, it is the responsibility of the programmer to insure that the IFDR is cleared before entering Copy Mode.

Copy Mode

When transmitting from the computer to the 7750, the latter, by setting the Service Request trigger on, will ask for a character every 14 microseconds provided the computer answers by turning on the Service Response trigger and placing a character on the Write bus within 6 microseconds after the request. Should the computer reply with a Service Response within the required time, the 7750 will normally transfer the character to the appropriate location in the Process Storage Data Register (PSDR), and proceed to the next character. When in Copy Mode, the 7750 will increment the W Address in the Control Storage Data Register (CSDR-W) after each transfer of a character from the IFDR to the PSDR.

During normal operation of Copy Mode, the CSDR-W will be placed in either Process Storage Address Register 2 or PSAR-1 in order to bring out of Process Storage the word into which the incoming character will be stored. The address register used is contingent upon the portion of the machine cycle during which the transfer takes place. Address transfer will not take place during Character Interrupt because the Character Bus is in use at this time.

Interruption or Termination of the In Operation

The normal transfer of characters into Process Storage may be interrupted or terminated for several reasons.

When the five low-order positions of CSDR-W become ones, the D character addressed contains the 11 high-order bits of the address of the next Block in the chain. These 11 bits are transferred to the high-order positions of the CSDR-W and PSAR-1, and the 5 low-order bits of CSDR-W and PSAR-1 are cleared. This procedure sets up the correct Process Storage location for the next incoming character at the loss of one storage cycle.

Simultaneously with the five ones test, the W Address and Limit of CSDR are compared. If the addresses compare, the allotted storage space has been exhausted and the present or any future character of this message will not be received, unless the programmer prepares a new chain for the remainder of the message. A successful comparison of the Address and Limit of the Copy Word in CSDR will set an Address Compare trigger, reset the Copy Mode Request trigger, and cause the IBM 7750 to go into In Mode.

The In operation will be terminated if the computer sends the Stop signal. When the Stop Signal occurs without a Service Response, the IBM 7750 will ignore any character sent at the same time the Stop signal is transmitted. Stop will reset Copy Mode Request, and cause the 7750 to revert to In mode. In this case, the In mode program will turn on the End trigger of the IFCR after it has completed the necessary housekeeping which normally follows the termination of Copy Mode. If the 7750 program detects that an Address Compare caused termination of the In operation (by the Stop trigger being off), the decision is left to the programmer whether the End trigger or the Unusual End trigger of the IFCR should be set at the end of In Mode housekeeping.

The IBM 7750 will exit from Copy Mode with the address contained in the CSDR-W equal to one character location more than the location of the last character stored. The Block Control Character is not considered a Character location in the chain.

The computer may send a Service Response and a Stop signal at the same time. In this case, the IBM 7750 will accept the character from the computer.

No character transfer, address incrementing, or address test can be performed during a Character Interrupt cycle.

A Copy Delay trigger is used to control the time at which Copy Mode operations are initiated and terminated. It delays the start of Copy Mode operations until a particular cycle time is reached and also delays the termination of Copy Mode into the next I cycle following the reset of the Copy Mode Request trigger. Prolonging Copy Mode operations at the termination of Copy Mode is necessary to complete the character transfer in progress. If Channel Service is requested, the Copy Delay trigger will delay the In operation until such time as the 7750 returns to Copy Mode to complete the In operation.

Copy Proceed and Inhibit Triggers

The IBM 7750 proceeds with the In operation by sampling the status of various triggers every 14 microseconds. The purpose of sampling is to control acceptance of characters from the computer to allow for conditions which interrupt character transfers. A Copy Proceed gate is used to control the sampling, which in turn determines any of the following conditions:

(a) The Character Interrupt trigger is on.

(b) The Service Request trigger is on. The computer has not answered the last Service Request.

(c) The Address Compare trigger is on.

(d) The Five Ones trigger is on.

(e) The Copy Mode bit of the MRR is off.

(f) The Z Timeout trigger is on.

If one or more of the above conditions exists, Copy Proceed will set the Inhibit trigger which will be used to stop the generation of various character transfer gates, the generation of the next Service Request, the incrementing of the CSDR-W, and the generation of various reset pulses. In this manner, the normal transfer of characters to Process Storage will be controlled.

In order to block incrementing the CSDR-W until the first character is accepted, the Inhibit trigger will always be on during the first half-cycle of In or Out operation. It can only be reset at Copy Proceed time during Copy Mode status if none of the six previously mentioned conditions are present. This prevents the IBM 7750 from proceeding with any character transfers until the condition causing the Inhibit has been removed.

If the Stop trigger of IFCR is on at Copy Proceed time, the Copy Mode Request bit of the MRR will be reset.

The Inhibit trigger controls gates used for character transfer. An exception is the gate from transferring the character address from CSDR-W to either PSAR-1 or PSAR-2.

Method and Conditions for Generating a Service Request

There are three separate conditions where a Service Request will be issued during Copy Mode for the purpose of requesting transmission of a character from the computer.

The 7750 will issue a Service Request at the start of a message due to a different set of conditions than during the message transmission. If the In Mode Request trigger is

on, and the Service Response trigger off, the Service Request trigger will be set on when the Copy Delay trigger is set on. This is the only circumstance under which a Service Request may be issued while the Inhibit trigger is on.

Service Requests will be made by the 7750 after each Copy Proceed if, at Copy Proceed, the Inhibit trigger was off and the Copy Delay trigger was on. No Service Request will be issued at any time if the IFCR Stop trigger is on during the time that the In Mode Request trigger is on.

If the Inhibit trigger is off during the time when the Copy Delay trigger is on, Service Response will be reset immediately after Copy Proceed, but before another Service Request is issued.

A Service Response or a Stop Signal will reset the Service Request trigger.

It is desirable to prevent the associated computer from tying up the 7750 in Copy Mode while the latter is waiting for a Service Response from the computer. The countdown counter in positions 11 through 1 (Z field) of the CSDR will be used to count the number of 7750 cycles which elapse from the time a Service Request is issued until the computer responds with a Service Response. The program will set all the Z field bits to logical Zeros before setting the Copy Mode Request bit of the MRR. The Z counter is decremented and then tested once each Copy Mode cycle. If all the bits in the Z field become logical Zeros before the computer responds with a Service Response or a Stop, the Copy Mode Request trigger of the MRR will be reset. The program will return to Out or In Mode, where it must determine the reason for leaving Copy Mode. The program will check the IFCR for normal completion of the mode. It can also check the Copy Word for an Address Compare or a failure of the computer to respond. Having determined the reason for leaving Copy Mode, the program will take the desired action.

The Out Operation: Transmission from the IBM 7750 to the Computer

The Out Mode Operation for Entry Into Copy Mode

The Out operation is similar to the In operation previously described, although the data flows in the opposite direction. Much of the logical circuitry is common to both operations. The Inhibit, Copy Delay, Address Compare, and Five Ones triggers are used for both operations. Reference will be made to the In operation when this will reduce repetition.

Transmission of data from the 7750 to the computer can be initiated by the 7750 program. The program brings up the Attention line to the computer via the Attention bit in the IFCR. The computer will then bring up the Attention Response line to the 7750, which resets the Attention bit. The computer must be programmed to bring up either the Read or Sense line to the IBM 7750. The Read line will set the Out bit of the Mode Request Register. The Sense line will set the Sense bit of the IFCR and the Out bit of

the Mode Request Register (MRR). See Figure 7. The output from the Out bit of the MRR is sent to the computer on the Command Response line. The subroutine for Out Mode will examine the IFCR to determine if the Sense bit is on. Sometime prior to entering Copy Mode, the program will have set up the Copy word with the Address (W) and Limit of the chain to be transmitted to the computer. The program will then set the Copy bit of the MRR, leaving the Out bit on. The Copy Mode has higher priority than Out Mode, and consequently the IBM 7750 will go into Copy Mode at the start of the next I cycle.

Copy Mode Character Transfer

When transmitting from the 7750 to the computer, the former, by turning on the Service Request bit will indicate that it has placed a character on the Read bus. This will be done twice every 28 microseconds providing the computer accepts characters at this rate, and providing the 7750 is not interrupted by such conditions as described for the In operation. The 7750 will test the Service Response trigger every half cycle for the existence of a Service Response. When the computer responds by accepting a character and giving a Service Response, the 7750 will transfer the next character from the Process Storage to the IFDR, and issue another Service Request.

Interruption or Termination of the Out Operation

The Out operation is terminated by circumstances similar to those in the In operation.

As in the In operation, a test is made on the Copy word for five Ones in the lower order bits of the CSDR-W. Similarly, the new Block location, in the case of a successful test, will be accessed from the PSDR while in Copy Mode.

A test is made for equality of the W Address and Limit of the CSDR, as in the In operation. If the addresses compare, the 7750 has transmitted the contents of the current chain, and the Copy Mode Request trigger will be reset, causing the 7750 to revert to Out Mode.

If neither the Address Compare test nor the Five Ones test is successful, CSDR-W is placed in PSAR-2 or PSAR-1 in order to access the Process Storage character which is to be transmitted to the computer. The character is taken from the PSDR, placed in the IFDR via the Character Bus, and the Service Request bit is turned on. The CSDR-W is again ineremented, and the previous two tests repeated.

The eomputer may terminate Out operation by sending a Stop signal which sets the Stop bit of the IFCR. The last character will be available to the computer on the Read bus at this time; the computer has the choice of taking or ignoring this character. The Stop signal will reset Copy Mode Request, and cause the 7750 to revert to Out Mode. The End or Unusual End triggers will then be set as was done for the In operation.

The 7750 will exit from Copy Mode with the CSDR-W equal to one character location further in the chain than the location of the last character transmitted. The Block Control Character is not considered a character location in the chain.

After a successful Address Compare, the 7750 will not exit from Copy Mode during the Out operation until the Service Response is received. This acknowledges that the computer has accepted the final character, which was on the Read Bus at the time. The Z field counter previously mentioned will prevent the 7750 from becoming stalled in Copy Mode for lack of a computer Service Response.

The computer can give either a Read or a Sense command to the 7750 without the 7750 giving a prior Attention signal.

A Character Interrupt, a mode change to a higher priority mode, or a failure of the computer to provide a Service Response signal within a specified time will insert delays between transmission of characters.

LOADING THE IBM 7750

Load Trigger and Load Counter

A Load trigger in the IFCR controls the loading and unloading of complete 48 bit words to and from Process Storage. This Load trigger can be set from the Load button on the Operator's panel or by the 7750 program. When this trigger is on, the 7750 responds to a Read, Write, Sense, or Control command from the computer in a manner different from that previously described. It will execute the Out or In operation normally except that 16 charaeters of 3 bits each will be stored in or transmitted from a single word. A four-bit Load Counter will be used to control the number of characters which can be loaded into each word. The 16 characters, which comprise one word, will be placed into or received from the 1, 2, and 3 positions of the IFDR and will be stored in or taken from PSDR positions 47-45, 44-42, 41-39, 38-36, 35-33, 32-30, 29-27, 26-24, 23-21, 20-18, 17-15, 14-12, 11-9, 8-6, 5-3, and 2-P under control of the Load Counter. When a complete word is assembled into the 7750, position P, the word parity bit, will be checked to ensure proper loading. The Load Counter is reset after each 16 count and when the Load bit of the IFCR is reset.

Loading Under Program Control

To load or unload the IBM 7750 by program, the IBM 7750 is put into In or Out mode in the same manner that was followed in the previous sections. When in Out or In mode, however, the appropriate program sets the Load trigger of the IFCR. The program then sets up the W address and Limit and turns on the Copy Mode Request trigger. Loading or unloading starts from the W address of the Copy Control word and continues

in sequential storage locations until the computer signals Stop (during Load) or the Limit and W address of the Copy word compare (during unload).

After a complete word has been assembled or transmitted from a given word address, the W address of the Copy Control word is incremented by 1 word location, or 4 character locations, in order to access the next word in Process Storage.

The 3-bit byte transmission is continued in the normal In or Out mode. No test for five-ones will be made when the Load trigger is on since it is necessary to store or access words from all addresses.

When loading or unloading is completed, the IBM 7750 proceeds to the program determined by the MRR.

Loading Under Manual Control

The IBM 7750 must be in a Program Stop status at the time the operator initiates a manual load. All triggers and registers can then be reset by utilizing the Reset Switch or the Clear Switch, depending upon whether the storages are to be cleared or to remain unchanged.

Pressing the Load button will then set on:

1. Load trigger of the IFCR
2. Manual Load trigger
3. Attention trigger of the IFCR
4. Mode Change trigger
5. Stop-Start trigger

The manual load trigger is kept on until the first word has been loaded or unloaded.

During the time when the Manual Load trigger is on and no Read or Write command is received from the associated computer, the Mode Change trigger will be kept on. This prevents the 7750 from executing instructions and, consequently, stopping due to an Op code parity error on the words which were previously reset. A Write command from the computer sets the In trigger of the MRR. Because the Manual Load trigger is on, the Copy Mode Request trigger will be set on immediately, allowing the Mode Change trigger to be reset. When the Copy P-Word is read out for the first time during manual Load, it is reset, so that loading starts from address zero in Process Storage. When the 7750 goes into In mode, the In mode P-Word is reset when first read out causing the In mode program to start at the instruction in address zero of the Process Storage.

The Address Compare for the first 16 characters is inhibited by the Manual Load trigger. This trigger is reset when the first word has been assembled into the PSDR.

When loading of sufficient instructions is completed, the IBM 7750 will revert to In or Out mode because of a Stop signal, Address Compare or Z timeout condition. Thereafter, any further loading will be under control of the instructions previously loaded.

During both manual and program loading operation, the 7750 continues its scanning of the Process Control Channels. The programmer must take precautions to ensure that the scanning does not interfere with the loading routine. The Control Storage must be loaded by the 7750 program, which also resets the Load trigger of the IFCR on completion of the loading routine. The Z counter operates in the same manner as for normal data transfers. That is, when the Z counter is decremented to all zeros it causes the 7750 to exit from Copy Mode. However, the Z counter will not cause the machine to exit from Copy Mode until the first word has been completely loaded under manual load conditions.

As in the normal data transfer operation while in Copy Mode only, In Mode or Out Mode may be requested at any one time, but not both.

PROGRAMMING ASPECTS

Z Timeout Trigger

During 7750 operation, it is desirable to prevent the computer or console from setting the Stop trigger in the IFCR when the 7750 is not in Copy Mode. This allows the programmer (by testing the Stop trigger) to get a true indication of the reason why the machine left Copy Mode. Otherwise, the Z counter may decrement to all Zeros and there is a remote chance that the Stop trigger may be set on after the 7750 leaves Copy Mode but before the programmer can test it. He might then draw an incorrect conclusion that the computer caused the exit from Copy Mode. The programmer may, consequently, branch to the wrong place in his program.

To ensure correct operation, the output of the Stop trigger is gated with the output of the Z Timeout trigger. This trigger is set on when a "Z-counter-all-Zeros" condition is detected. It is turned off whenever Stop or Service Response are on during any of the succeeding times when the machine re-enters Copy Mode. While the trigger is on, the output of the IFCR Stop trigger is de-gated to the character Bus, thus making it appear to the programmer that the Stop trigger is not on.

If the programmer finds the Stop trigger off after exiting from Copy Mode, and no address compare occurred, then he assumes that the Z counter decremented out. Should Stop come after the Copy Mode exit, the programmer can do one of two things:

a. He can set Copy Mode Request and will accept one character before exit again.

b. He can give End or Unusual End to the computer if he knows by system operation that the "Z counter = 0" signal means an inoperative computer. (In the case of the 7750 console, the Z counter may decrement to zero many times between cards even though the card reader is operational). In this case the computer End Response will reset Stop and the Z Timeout trigger.

Copy Address Compare and "Five Ones" Simultaneously

A problem arises when the programmer wishes to exit from Copy Mode because of an address compare and he wishes to store all 31 characters in the last Block. He cannot place an address with 5 low order ones on the Limit unless he chains onto this last storage Block another Block from which to get the new W address since it is necessary to exit from Copy Mode with the W address one more than the location of the last character stored. (And the Block Control Character is not considered to be a position in the Block). Under these conditions the W address at the time Copy Mode is finished cannot be predicted.

A solution to this problem is to place all zeros in the Block Control Character of the last Block and make the Limit all zeros. When the "five-ones" condition occurs, the D field will be accessed and will set the W address to zero also. The zeros in both addresses give an address compare and cause a correct termination of Copy Mode.

Interface Parity

The 7750 computer interface uses ODD parity. This odd parity is generated in the high order bit of the IFDR when the 7750 is unloading. When BCD or other character codes are being sent on the Read Bus, the 7750 program will insert the odd parity bit. No parity check is wired in for incoming characters on the Write Bus. However, as mentioned in the section on loading, a parity check is made on all 48 bits when the 7750 has completed the loading of a full word.

Continuous Read or Write of One Storage Location

A method exists in the Copy Mode controls for continuously reading and writing one address in Process Storage. The programmer may execute this type of an operation for diagnostic purposes by setting up a Copy P-Word such that the Z field contains logical Zeros in all but the low order bit position,which has a logical One. The contents of the W address will be the storage address to be used. The programmer will then set on the Copy bit of the MRR leaving the In and Out bits OFF. This forces a Z timeout on the first cycle and the Z timeout trigger can then be used to hold the Inhibit trigger on during subsequent times that the program re-enters Copy Mode. The advantage of such a system is that two storage accesses per 28 microsecond cycle are possible, significantly faster than the same operation carried out by 7750 instructions only. No Service Request will be given to the computer by this method.

Use of Address Compare

This section discusses the usage of Address Compare for Copy Mode termination. First, for In Mode, if the addresses compare and the allotted storage space has been exhausted, the present and any future characters of this message will not be received, unless the programmer prepares a new chain for the remainder of the message. The "present" character means that a Service Request is issued by the 7750 at the time when it finds that the Limit and W address compare. If the computer or console send a Service Response, then any information sent will not be accepted by the 7750. This extra Service Request may be prevented only if the computer or console gives a Stop, delayed by no more than 4 microseconds from the time that the previous Service Response was sent.

A more difficult situation develops when the programmer attempts to terminate the output transfer of characters from the 7750. In order to transmit to computers at a maximum speed of 2 characters per machine cycle, it becomes necessary to set up the next Process Storage address before the Service Request for the previous character has been sent. Consequently, when a computer or console sends a Service Response followed by a Stop, two address increments may take place after the last character was sent. It is, therefore, inadvisable to permit this type of termination of output operations. Alternatively, the operation should be terminated by one of the following methods:

A. Address Compare

B. Stop issued during the time Service Request is on and not accompanied by a Service Response.

ERROR CHECKING

Checks

1. Full Word Transfer Check -- When full words are transferred between Control Storage Data Register and Process Storage Data Register, the parity bit P is also transferred and an odd parity check is made on the word in each register.

2. Parity Check -- Process Storage and Control Storage have a parity bit P associated with each word. Before writing into either storage, P is generated so that the word has odd parity. An odd parity check will be made after reading a word from either storage.

3. Instruction Register Parity Check -- An odd parity check is made on the Op code, bits 1-10, and Flag data, bits 12 and 13, of the Instruction Register and the parity bit. Bit position 11 is the parity bit located in Process Storage Data Register, and will be generated by the assembly program or whenever any changes are made in this field of the Instruction Word.

4. Clock Check -- The clock in the IBM 7750 is checked for (a) multiple pulses or (b) no pulses.

5. Channel Check -- There are 16 Channel Check lights mounted on the operator's panel, one for each 7750 Process Control Channel. Since each high speed communication channel is connected to one 7750 Process Control Channel through a high speed channel adapter, each light numbered represents a corresponding high speed communication channel. Therefore, if a Channel Check light goes on, it means that a channel error has occurred in the high speed channel associated with that light.

For low speed operations, when a Channel Check light goes on, it indicates that a data transfer error has occurred on one of the low speed channel communication channels attached to the MCA; or that an MCA storage parity error has occurred. However, the number of the Channel Check light is not associated with the low speed communication channel in error but with the MCA it is connected to.

Error Proeedure

The error procedure is to set the error trigger and to either request Service Mode or stop the machine. Two types of errors, clock check and instruction parity check, will always stop the machine. A channel check will always request Service Mode. The remaining checks, full word transfer check and parity check (PS or CS), can stop the 7750 or request Service Mode. Whether to stop the machine or request Service Mode depends on the position of the Check Switch on the operator's panel. If the Check Switch is set to the Service position, the 7750 will go into Service Mode when either one of the two errors occurs.

The Full Word Transfer, Process Storage Parity, Channel Check, and Control Storage Parity Check triggers are actually part of the Channel Service Register. Program instructions can store or reset these positions. If it is desired to bring the 7750 to a Program Stop status while the Check Switch is set to Service position, the program must execute an instruction which contains an even parity configuration in the Op Code and Flag data field.

If the Check Switch is set to the Stop position, the Full Word Transfer Check, and the Process Storage or Control Storage Parity Check can set their respective triggers when a corresponding error occurs. However, the IBM 7750 clock will continue to step. Towards the end portion of the Execute cycle, provided a Character Interrupt or the second Execute cycle of a two-cycle instruction is not being processed, the Start/Stop trigger will be set to Stop status. With the Start/Stop trigger on Stop status, the IBM 7750 clock will stop within the Instruction cycle of the next machine cycle.

When a clock error is deteeted, the 7750 will reset the clock immediately. When an instruction parity check is detected, the instruction will be extended and the stop trigger set on, causing a normal machine stop at the end of the instruction. In all cases, when one of the errors discussed above occurs, the corresponding check trigger is set and a check indication will appear on the operator's panel.

OPERATOR'S PANEL

The Operator's Panel (Figure 16) contains the following three groups of switches and lights.

Power Controls and Indicators

Switches	Lights
	Thermal
Power Off/Power On	Power On
DC On	DC On
DC Off	Circuit Breakers
	Blower

Control Switches

The Stop Switch sets the Stop/Start trigger to Stop status at the end of execution time of a machine cycle provided the 7750 is not processing a two cycle instruction or a Character Interrupt. If either one of these conditions exists, the IBM 7750 clock will continue to step until the two cycles instruction or character interrupt is completed.

When the Start/Stop trigger is set to Stop status, the clocks will continue to step until the early part of I time of the next machine cycle.

The Start Switch starts the clock and resets all check triggers. The IBM 7750 must be in Program Stop status for this switch to be effective.

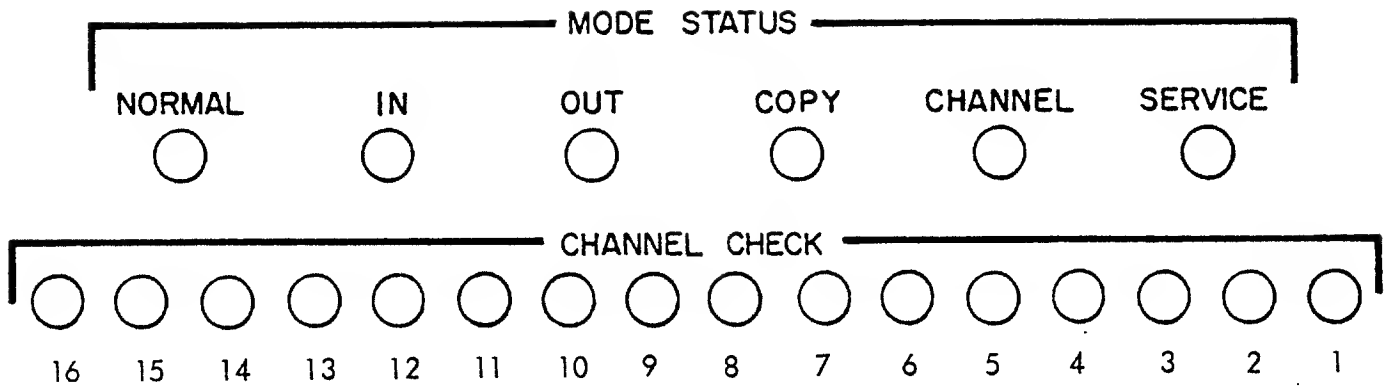
The Reset Switch generates a manual Power-On-Reset. The IBM 7750 must be in Program Stop status for the switch to be effective.

The Clear Switch clears both Control Storage and Process Storage and resets all registers and triggers. The IBM 7750 must be in Program Stop status for the switch to be effective.

The Service Mode Switch sets the Service Mode trigger on provided the 7750 is in Automatic status.

The Load Switch sets the Load trigger in the Interface Control Register enabling the associated computer to load the 7750. The 7750 must be in Program Stop status for this switch to be effective.

The Channel Reset Switch resets all Channel Check indicators.



CIRCUIT BREAKER	THERMAL	BLOWER	CHECK	CE TEST			CLEAR
POWER ON	DC ON LIGHT		SERVICE MODE	SERVICE CHECK STOP	LOAD LIGHT	AUTOMATIC	PROGRAM STOP
ON POWER OFF	DC ON	DC OFF	RESET	CHANNEL RESET	LOAD	START	STOP

FIGURE 16 OPERATOR'S PANEL

The Check Switch, when set in the service position, causes the 7750 to enter Service Mode when certain checks occur. When this switch is set to the Stop position, the 7750 will go to Program Stop status when certain checks occur.

Operation Monitors

The Load Light indicates that the IBM 7750 is loading when the light is on.

The Automatic Light indicates that the IBM 7750 is under the control of its own program.

The Check Light goes on whenever an error occurs in the Process Control Rack.

The Channel Check Lights, one light for each channel, indicate that a channel error has occurred.

The Mode Status Lights, one for each mode, indicate which mode the 7750 is in.

The Program Stop Light goes on when the IBM clock stops.

The C. E. Test Light goes on whenever the IBM 7750 is in C. E. Test Status.

CHANNEL ADAPTERS

The eommunieations system of a eustomer may be comprised of a number of different types of communieations serviees. For cxample, there are telegraph machines, operating at 60, 75, and 100 wpm, employing both polar and neutral signaling. A variety of digital subsets, made by the eommunications companies, are used. Few of these deviees employ the same signal levels, or bit rates, but they must all be integrated into many TELE-PROCESSING systems. In order to economically join the IBM 7750 to a eustomer's system, various channel adapters are used.

These ehannel adapters, aecording to type, perform a variety of funetions. Some types of channel adapters eontrol digital subsets, while others time-multiplex a number of low speed communieations ehannels into one or more high speed channels.

Thc principles underlying the design of the various adapters are those of providing flexibility to meet the needs of thc customer, while taking advantage of the power of a stored program processor, to reduce the eost and complexity of the equipment per communieations line.

TYPE 1 MULTIPLEXING CHANNEL ADAPTER

The Type 1 Multiplexing Channel Adapter (MCA1) is a ehannel eoneentrator, and speed changing device. It derives data from a number of ineoming channels by a scanning and sampling teehnique, and transfers this data, together with timing whieh it generates, to the Proeess Control Rack. The MCA1 aeeommodates up to 28 low speed, half-duplex channels plus 1 test ehannel and eommunicates with the Process Control Rack via one or more high-spced eommunieations ehannels. The maximum bit rate on a channel conneetcd to an MCA1 is dependent on the number of low speed ehannels into the MCA1, the number of high speed ehannels into the Process Control Rack,and the number of Process Control Rack ehannels to which the MCA1 is eonneeted.

The low speed ehannels are divided into Low Speed line adapter sets of four channels each and all ehannels within a set must operate at the same bit rate.

There are a total of seven sets available per MCA1. The bit rate per feature may be any value up to the limits imposed by Tables 13 and 14. The bit rate per set is controlled by a sample cloek oscillator (SCO). Eaeh set may be controlled by a different SCO or any eombination of the seven sets using the same SCO may be used if the bit rate limits of the above mentioned tables are not exceeded. The bit rate for any set can be field ehanged.

Equipment Configurations

The MCA1 is made up of several basic pieces of equipment. They are: the low speed basic equipment package, the Multiplexor Storage Data Register with its controls, and the Transmit-Receive Scanner equipment. The basic equipment package contains hardware used in conjunction with other MCA1's. As many as 4 MCA1's can be attached to the basic equipment package.

If a second MCA1 is added to a 7750 already containing one MCA1 with its basic equipment package, some additional circuitry will be required in the basic package plus the addition of a storage data register with its controls and Transmit-Receive Scanner equipment. Each MCA1 controls seven sets (four communication channels to a set) plus one test channel. Since one 7750 can be connected to four MCA1's, it can serve a total of 112 low speed communication channels and 4 test channels.

The equipment configuration for the 7750 was chosen to realize the advantages and accompanying cost reduction of using common circuitry in certain portions of all multiplexing channel adapters. All MCA1's which share a portion of the low speed basic equipment package operate in synchronism. Because of this, all such MCA's must scan the same number of channels, although it is not required that all channels be utilized in each MCA1. In general what occurs in one MCA1 can be assumed to happen in each of the other MCA1's which share the basic equipment package.

General Operation

The MCA1 operates with both the Process Control Rack and the communication channels on a bit by bit basis. That is, the MCA1 sequentially scans the communication channels, obtains bits one at a time from each channel, stores them in a buffer, and later transfers them at the proper time to the Process Control Rack. On transmission, the MCA1 takes bits one at a time from the Process Control Rack, stores them, and at the proper scan time for the particular channel, transmits the bits one at a time to the proper remote terminals. The transfer of bits between the MCA1 and the Process Control Rack is by demand from the MCA1. Bits are obtained from the channels and transferred to the Process Control Rack in the following way:

The MCA1 scans each of the communication channels for 14 usec every 14 n usec, where n = number of low speed channels connected to the MCA1. The scanning is done at a rate which insures that at least 10 scans will be taken, and thus 10 samples can be taken during a bit time for the fastest bit rate into the MCA1. This, then, is the relationship between the number of low speed channels into an MCA1 and the maximum bit rate on any low speed channel. The particular scans during which data samples are to be taken are controlled by a channel timing circuit. Associated with each speed group of low speed channels is a channel timing circuit, whose binary output changes exactly ten times during a bit time for the rated speed of this group of low speed channels. If during the scan of a particular channel, the output of the channel timing circuit is

different from its state during the previous scan of this channel, a data sample is taken and a sample counter is incremented. Similarily, consecutive scans determine additional samples until sample count 6 is reached. The sample at count 6 is taken as the value for this bit and is stored in the MCA1. Also, during sample count 6, a timing bit associated with this low speed channel is complemented. At some subsequent scan, prior to the following sample count 6, the Process Control Rack senses the reversal in the Timing bit for this channel, and accepts the bit stored in the MCA1 for this low speed channel as the next bit from the channel. The sample counter is reset on either sample count 10, or a detection of a level change in the sampled data.

On output, the MCA1 always transmits to low speed channels on sample count 6, and the sample counter is reset on count 10, except when elongated stop bits are to be sent. In the latter case, the counter is not reset on ten but on a count equal to the number of tenths desired in the stop bit, e.g. 14 for teletype. This number can be assigned any value between 1 and 1.5 integer bit periods by pluggable pins on a circuit card. Between consecutive counts of 6, the MCA1 obtains a new bit from the Process Control Rack. The exact scan time depends on the position of the precession of the Process Control Rack scan with the MCA1 scan.

Distortion

Receiving distortion is the percentage by which the actual bit width varies from that of the perfect bit width at the Communication Line Terminator Interface. In receiving, several types of distortion must be considered. However, in general, distortion due to transmitting speed can be separated from distortion due to lengthening or shortening of bits. Due to sampling methods used in the 7750, speed variations are more significant when trying to receive a large number of consecutive identical bits. The following two formulas may be used to compute the allowable distortion due to both speed variation and other types of distortion.

1. $0.3996 - .001N = L$

2. $0.5005 - .001N - \frac{2.01P}{B} = S$

where

N = Number of consecutive identical bits
B = Normal bit period
P = Normal scan period for the channel of the MCA1. This is equal to (number of channels scanned by MCA1) x 14 us.

Formula one gives the percentage of one normal bit period that may be added by distortion to N consecutive identical bits before a sampling error will occur. This percentage is L. Formula two gives the percentage of a normal bit period that may be subtracted by distortion from N consecutive identical bits before a sampling error

will occur. This percentage is S. Note that S is dependent upon the number of channels scanned by an MCA, and upon the normal bit period. To clarify the use of these formulas, consider the following example:

Transmission rate 75 bits/second
MCA1 scans 25 channels
Bits may be lengthened or shortened due to bias distortion of 20%
N = 6

therefore

$$L = 0.3996 - .006 = .3936 \cong 0.39$$
$$S = 0.5005 - .006 - 2.01 \times 7.5 \times 2.5 \times 1.4 \times 10^{-3}$$
$$S = 0.5005 - .006 - .0528 = 0.44$$

Since bias distortion may account for 0.2 bit width variation, this must be subtracted from L and S to find what distortion can be introduced by speed variations.

therefore

$$L = 0.39 - 0.2 = 0.19$$
$$S = 0.44 - 0.2 = 0.24$$

The speed tolerance can now be found by dividing L and S by 6, the number of consecutive identical bits which are to be properly sampled. Therefore, each transmitted bit must be written its normal length by

$$1 + \frac{.19}{6}$$

$$1 - \frac{.24}{6}$$

or the bit may be varied from 1.03 to .96 of its normal width. Regardless of transmitting speed and the number of channels scanned by an MCA1, the worst case condition occurs when P = 0.1 B. This condition implies that in the worst case, no single bit may be lengthened by more than 40% or shortened by 30%. Note that in actual practice, P is generally much smaller then 0.1 B.

When transmitting from an MCA1, the following distortion formulas give the amount, in fractions of a normal bit width, by which a group of consecutive identical bits may be lengthened or shortened.

Amount group lengthened = 0.001 NB + 1.005 P
Amount group shortened = 0.001 NB - 1.005 P

where

N = Number of consecutive identical bits
B - Normal bit period
P = Normal scan period for this channel of the MCA1. This is equal to (number of channels scanned by MCA1) x 14 us.

The worst case occurs when P = 0.1B. In most systems P will be much smaller. A single bit may vary, from about 90% of its normal length to about 110% of its normel length.

DETAILED DESCRIPTION

The MCA1 is divided into six functional units (Figure 17):

(1) Address Register
(2) Channel Scanner
(3) MCA1 Buffer
(4) Multiplexor Storage Data Register
(5) Data Control
(6) Adapter Control Interface

Address Register

The address register is a five stage binary counter used for sequential addressing of the communication channels. The register's binary output, together with two wired-in bits, supply the 7 bit address sent to the process control rack for addressing control storage during a scan cycle. The value of the wired-in bits depends on which MCA1 (A, B, C, or D) is being used. When decoded into a 4 out of 32 output, the Address Register addresses the MCA1 buffer X read-write drivers, X gates, Y read-write drivers, and Y gates. Also when decoded into a 2 out of 12 output, the register addresses each of the MCA1 scanners simultaneously. The 2 out of 12 output is obtained by decoding the first two positions of the counter to determine 1 of 4 possible outputs. The remaining three positions are decoded to determine 1 of 8 possible outputs. The 1 of 4 output serves as the Y address for the channel scanner matrix; the 1 out of 8 output serves as the X address for the scanner matrix. The X address also divides the 29 possible channels into sets of four channels each with the exception of the test channel; thus, the X address gates the appropriate channel timing circuit into data control. The address of the test channel is always 34 octal in each MCA1 and the speed of its channel timing circuit is selected by a switch on the Communication Line Terminator (CLT).

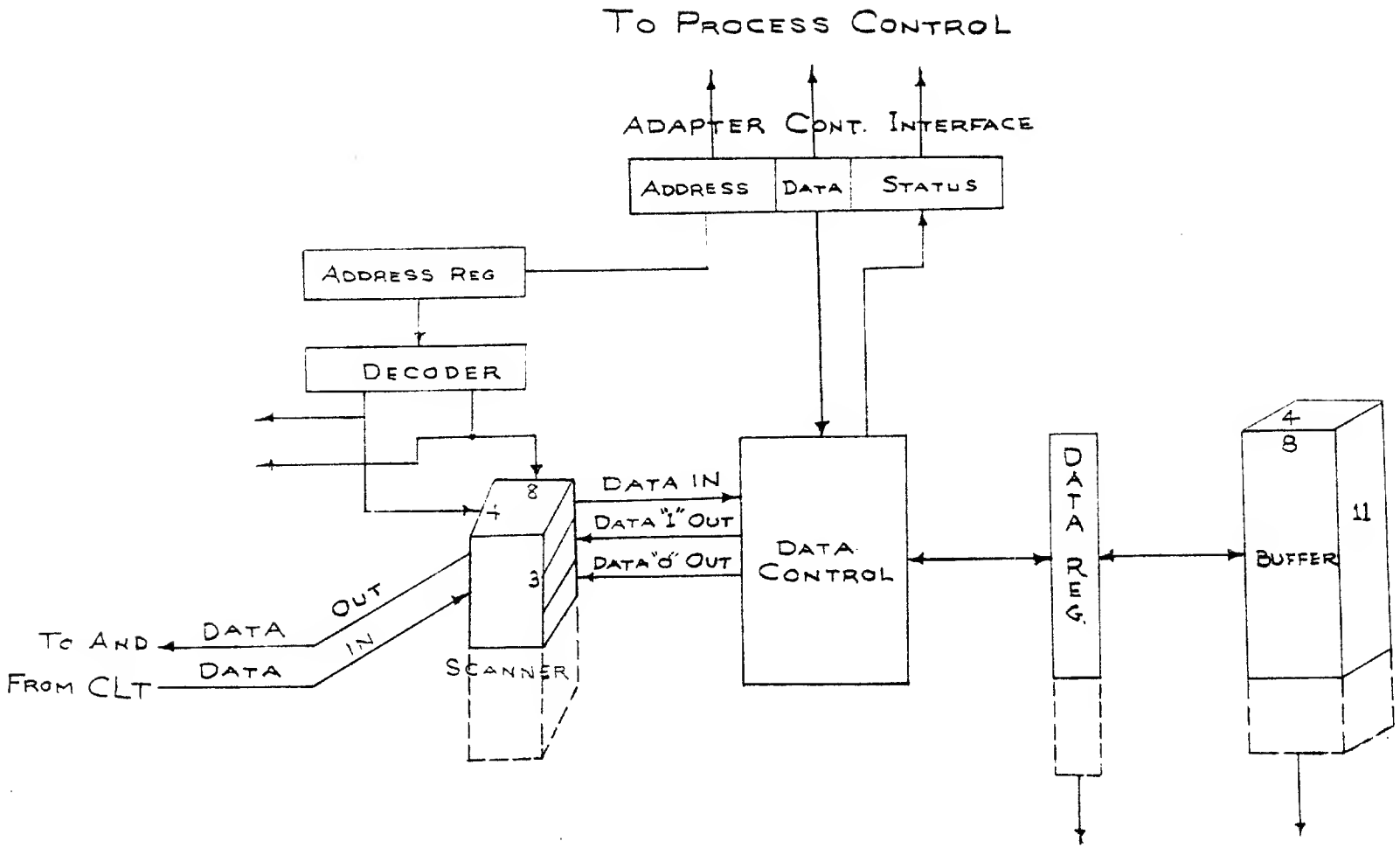


Figure 17 MCA1 Block Diagram

Channel Scanner

The channel scanner is a 4 x 8 x 3 matrix of AND gates conditioned by the decoded output of the address register. It is used for routing the input and output data between CLT and the MCA1's Multiplexor Storage Data Register (MSDR). Figure 18 shows the addressing, and gives an example of channel assignment. If less than 28 channel plus 1 test channel are scanned, the assignment of matrix points may take an even number of sequential addresses beginning with zero. Provisions are made to change the number on which the address register resets and the number to which it resets, according to the number of channels to be scanned. The address register automatically skips to the test channel from the last communication channel scanned and then resets to address zero. Each point in the matrix consists of three AND gates, one each for routing Data Out = 1, Data Out = 0 to CLT via Output latches, and Data In.

MCA1 Multiplexor Storage

The MCA1 Multiplexor Storage (MS) is a 32 word, 4 characters per word, 11 bits per character, core storage buffer which stores Multiplexor Control Characters -- one for each communication channel connected to an MCA1. The first character of each MS word is reserved for channels connected to MCA1-A. The 2nd, 3rd, and 4th characters of each word are reserved for channels connected to the respective second, third, and fourth MCA1's possibly associated with a 7750 Programmed Transmission Control System.

Multiplexor Storage Data Register

The Buffer Data Register is an 11 bit register from which multiplexor control characters are accessed. Associated with each of the communication channels connected to the MCA1, there is a multiplexor control character which stores the information required for the data derivation and multiplexing process. The multiplexor control character contains a single bit of data buffering, plus nine control bits used by the MCA1 to control the transfer of data to and from the communication channel. An eleventh bit provides character parity. Format of the multiplexor control character is as follows:

Bit Name	Number of Bits	Position
Data Bit	1	1
Last Data Sample (LDS)	1	2
Send/Receive (S/R)	1	3
Last Clock Sample (LCS)	1	4
Sample Counter (SC)	4	5-8
Timing	1	9
FSB	1	10
Parity	1	11

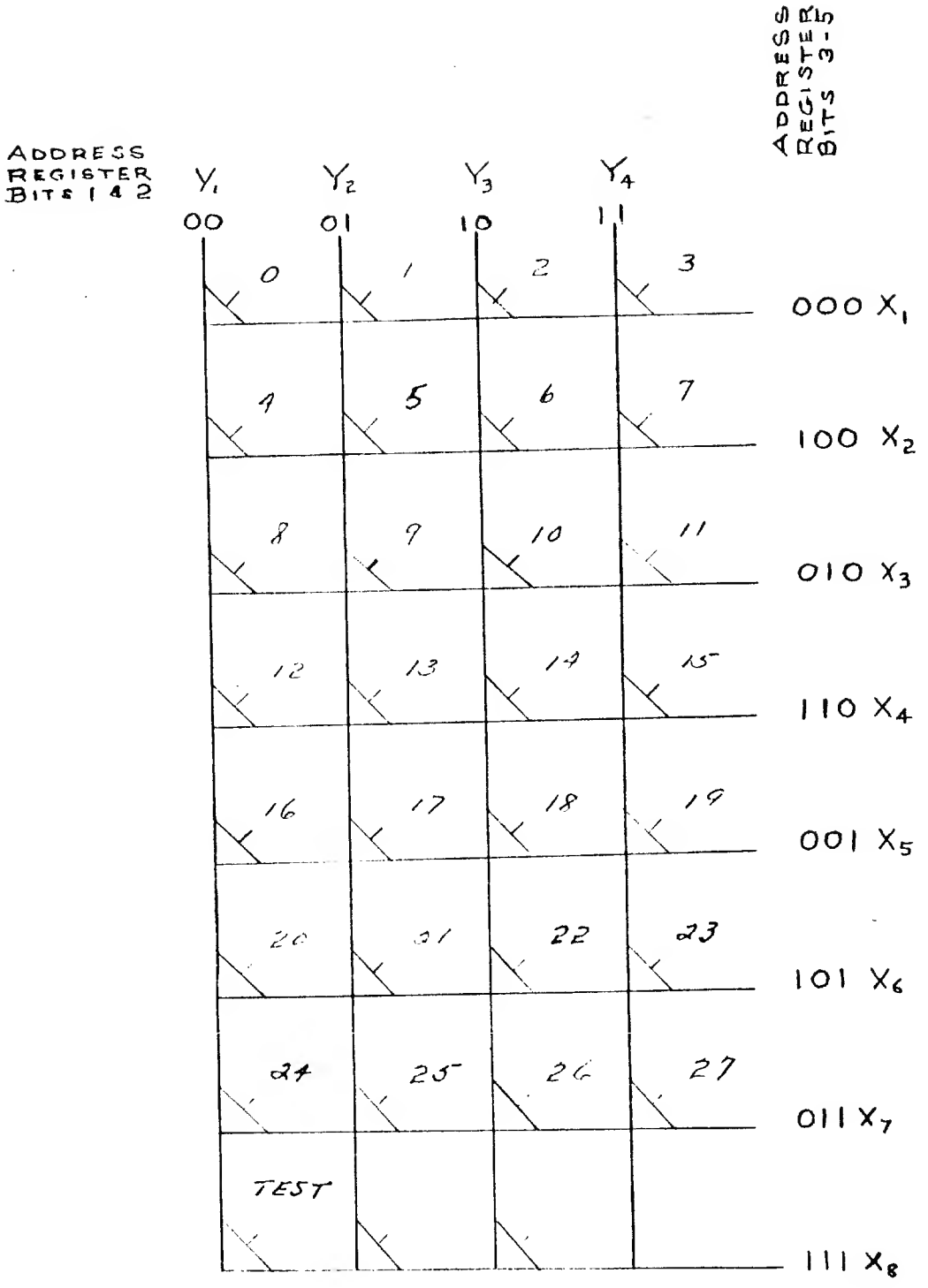


FIGURE 18 MCA1 SCANNING MATRIX

The functions of these bits are described below:

1. The data bit is a single bit used to buffer the asynchronous transfer of data into and out of the MCA1.

2. The last data sample in receive operation stores the previous data sample from the channel. In send operation, it is used to store the value of the data in the channel output latch.

3. The Send/Receive Bit controlled by the Process Control Rack tells the MCA1 the transmission status for this particular channel.

4. The Last Clock Sample Bit stores the status of the Channel Timing Circuit for this line during the previous MCA1 scan for this channel.

5. The Sample counter is a four stage binary counter which is incremented upon a detection of a change in status of the Channel Timing Circuit. Reset of the counter is caused by any of these four conditions:

(a) change in the S/R bit
(b) transition in the sampled data
(c) count of ten
(d) count of n

6. The Timing Bit furnishes line timing status to the Process Control Rack for the channel associated with this multiplexor control character. In particular, the bit is complemented on each count six of the sample counter.

7. The FSB Bit is turned on by Process Control for a channel in send status to cause the MCA1 to elongate the stop bit being transmitted to the Start-Stop Terminal connected to this channel. The FSB Bit is turned on by Process Control for a channel in receive status to degate the complementing of the Timing Bit when Process Control has received a complete character.

8. The Parity Bit provides character parity for checking buffer storage operation. This parity bit is used to generate odd parity before writing into storage and is checked at the end of every read time.

Data Control

Data Control is the miscellaneous control logic with which the MCA1 integrates the previous four sections to perform the required functions of channel scanning, channel timing generation, and data transfer to and from the communication channel and the Process Control Rack.

Of particular significance in Data Control are the Channel Timing circuits. Associated with each group of common speed channels is a Channel Timing Circuit whose binary output level changes ten times during a bit time (for the rated speed of the channel). The Channel Timing Circuit consists of a highly stable oscillator connected to a driver which

drives a binary trigger whose output is changing at a constant rate -- exactly ten times per bit period. Each level change in the trigger's output is interpreted as a sample time and ten samples are counted as a bit time. Thus if the channel is operating at exactly its rated speed, there will be exactly ten samples taken during a bit time. Should the channel be operating at some speed slightly slower than its rating, the ten samples per bit would be taken in a bit period of time less than the actual bit time which was transmitted. If several consecutive identical bits, say 14, were transmitted at this slower speed, it is possible that 15 bits would be derived from the channel instead of the correct number of fourteen. To prevent such inaccuracies from occurring, the 7750 must perform within certain transmission speed tolerances. See Section on Multiplexing Channel Adapter.

MCA1 OPERATION

The MCA1 derives bits from the lincs by a scanning and sampling technique. The scanning operation is performed synchronously with the Process Control Rack and asynchronously with the communication channels; however, the sampling operation is asynchronous with both the Process Control Rack and the communications channels. Sampling is done at a rate which insures that ten samples will be taken with sufficient accuracy to permit terminal distortions as dcscribed in the Section on Distortion. Since sampling is performed asynchronously, it follows that data transfers to and from the MCA1 are asynchronous; thus, a multiplexor storage is needed.

To explain the detailed operation of the MCA1, the following symbols are defined:

I	No. of Scan Points connected to the Process Control Rack (PCR).
N	No. of PCR scan points to which an MCA1 is connected.
i	No. of PCR scans between consecutive scans on a particular MCA1.
n	No. of low speed channels connected to MCA1.

Two 14-microsecond scan cycles of the MCA1 are performed during one scan process cycle sequence of Control Storage. The relationship of these cycles is shown in Figure 19. It can be seen that on alternate scans of the MCA1, the Control Storage is in a Scan Cyclc. On each i^{th} Scan Cycle of the Control Storage one of the N channels to which the MCA1 is attached is being scanned by the process Control Rack. It is during these coincidences of scan cycles that data may be transferred to (or from) the Process Control from (or to) the multiplexor control character associated with the communications channel being addressed by the MCA1 Channel Scanner. For simplification, i is assumed to be constant in this section; that is, the MCA1 is connected to the Process Control Rack channels which are evenly spaced.

The 14 microsecond scan cycle per line is divided into three phases as shown in Figure 19. In general, phase 1 consists of reading out the multiplexor control character for a particular MCA1 channel address. Phase II consists of modifying the control character as required and initiating data transfers to and from CLT and PCR. Phase III consists of writing the modified control character into multiplexor storage.

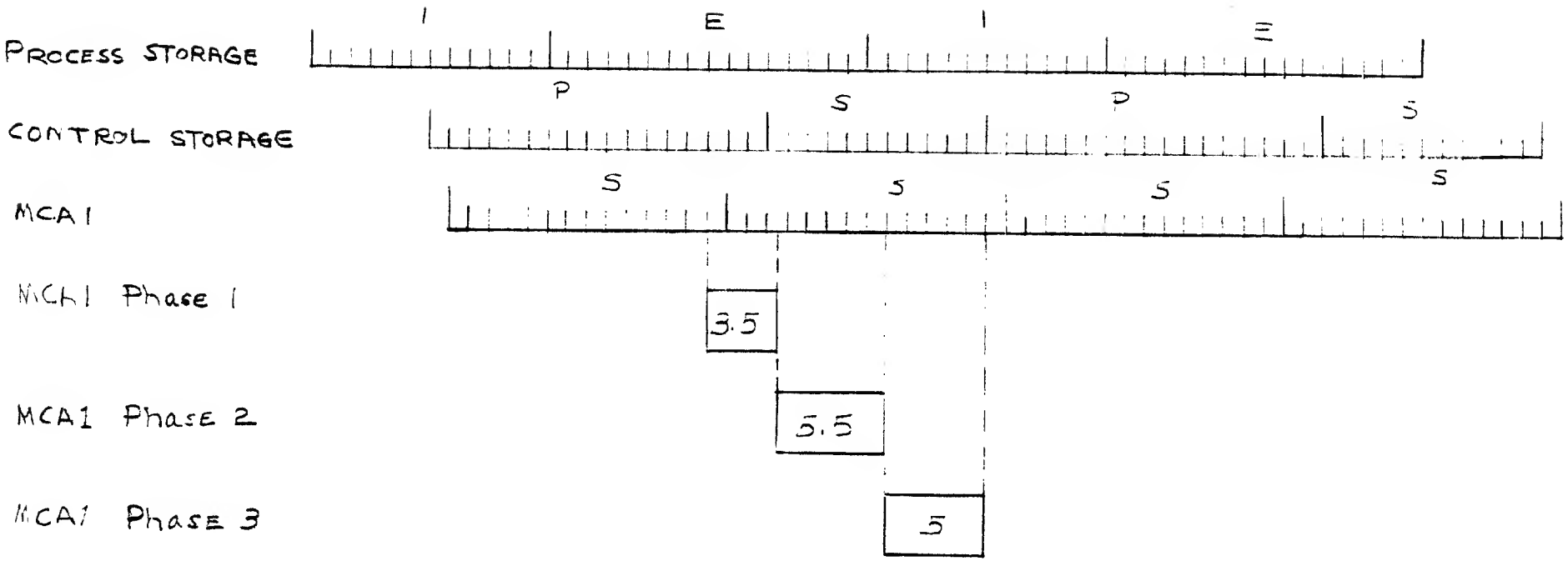


FIGURE 19 PROCESS CONTROL RACK - MCA1 CYCLE RELATIONSHIPS

TIMING

The PCR performs a 10 microsecond scan every 28 microseconds. The MCA1 performs two 14 microsecond scan cycles every 28 microseconds. Thus the MCA1 scans two low speed channels while the PCR is scanning one high speed channel. In addition, the MCA1 is connected to N Scan Points of the PCR and these N Scan Points are spaced i Scan Points apart in the scanning sequence.

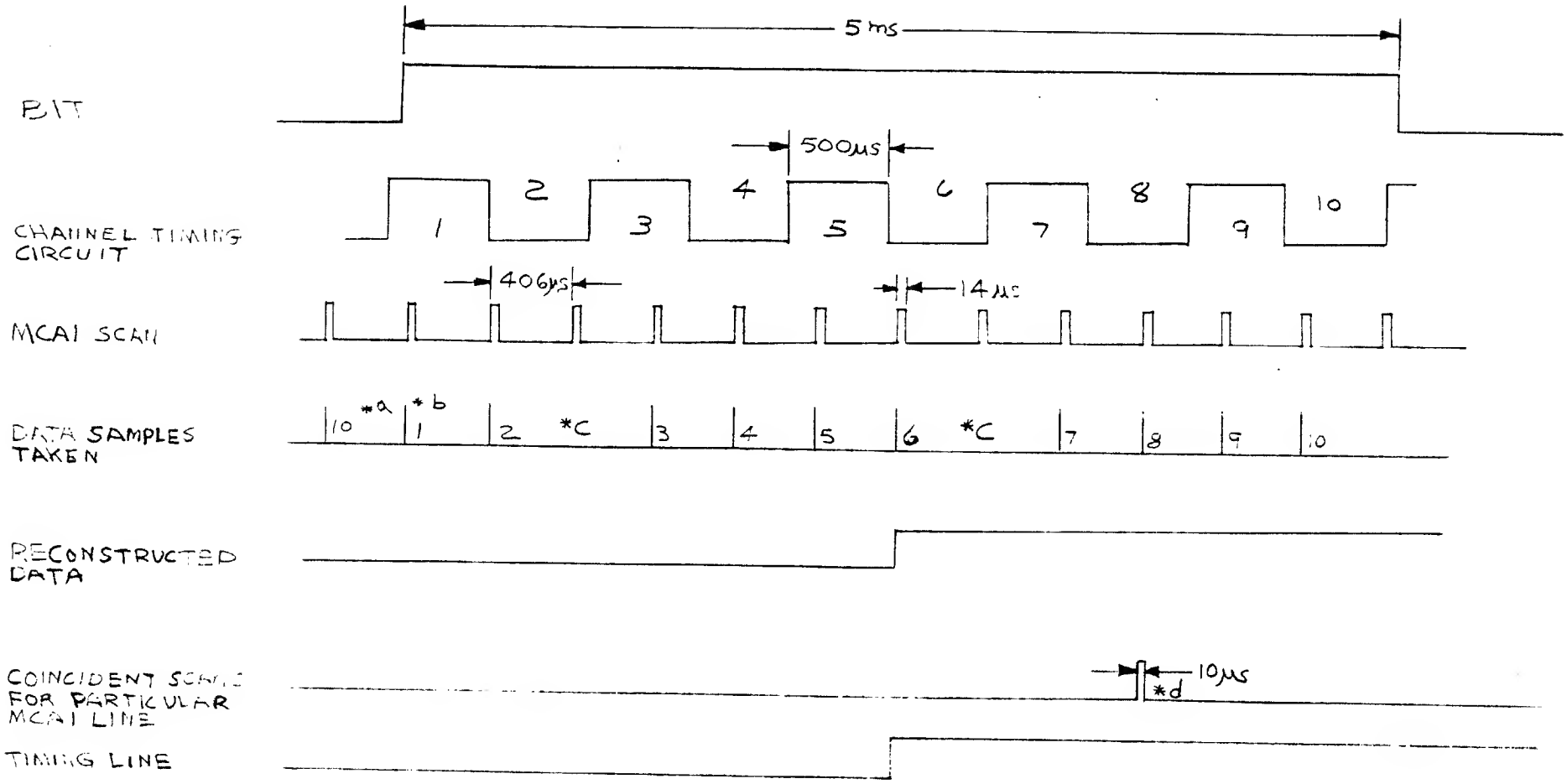
To facilitate explanation of the timing relationships between the PCR MCA1 and communications channels, a specific example will be used where I = 15, N = 3, i = 5, and n = 29. It will also be assumed that the maximum bit rate on any communication channel into the MCA1 is 200 bits per second (bit period of 5 msec.). Figure 20.

It can be seen from Table 7 that the MCA1 goes through ten complete scanning sequences of the 29 channels between times that the PCR sees a particular MCA1 channel.

With the maximum bit rate of 200 bps or the minimum pulse width of 5 ms., with 10 channel timing circuit transitions taken within each bit time, and with the relationships given in Figure 20 showing that the MCA1 scans a particular communications channel every 406 microseconds, it is assured that a scan, and thus a sample, can be taken at least once during each channel timing circuit period of 500 microseconds.

Furthermore, it can be seen that the PCR scans a particular low speed channel at least every 4.06 milliseconds and that every channel will be scanned by the PCR at least once during every bit time.

Since transmission is asynchronous to the IBM 7750, the beginning of a bit time can occur at any point with respect to the beginning of the timing chart of Table 7. For purposes of explanation, it will be assumed that the beginning of a bit time for low speed channel 10 occurred at microsecond 105. This new bit will be recognized at time 140 when the MCA1 next scans channel 10, and sample 1 will be counted. Succeeding samples are counted at times 546, 1358, 1764, and 2170 until sample 6 is counted at time 2576. At sample 6, data is taken from the channel and stored in the data bit of the multiplexor control character and its timing bit is complemented. At time 3794, the PCR is scanning this MCA1 and the MCA1 is scanning low speed channel 10. Thus the PCR sees low speed channel 10. Since the timing bit for this channel is different from the last timing bit in the channel control word for this channel, the PCR knows that a new data bit is stored in bit 1 of the multiplexor control character and it accepts this as a new bit from this channel. Since the PCR sees a given low speed channel every 4.06 milliseconds (less than minimum bit time), it is possible, by virtue of the asynchronism just explained, to see a particular bit twice. However, the bit is not accepted the second time since the timing line is not reversed. All clock timing signals needed in the MCA1 other than the Channel Timing Circuits are supplied by the central clock in the PCR.



*a COUNTER RESETS ON COUNT 10
*b NEW BIT DETECTED SINCE SAMPLE LEVEL IS DIFFERENT
*C NO SAMPLE TAKEN BECAUSE SCO LEVEL HAS NOT CHANGED
*d DATA TRANSFERRED TO PCR

FIGURE 20. TIMING RELATIONSHIPS
(FOR A CHANNEL IN RECEIVE STATUS)

TABLE 7 PROCESS CONTROL RACK-MCAI SCANNING RELATIONSHIPS

A	B	C		A	B	C		A	B	C		A	B	C		A	B	C		A	B	C		A	B	C		A	B	C		A	B	C	
1	14	1	OX#	1	420		O	1	826	15	O	1	1232		O	1	1638	14	O	1	2044		O	1	2450	13	O	1	2856		O	1	3262	12	O	1	3668		O	1	4074	11	OX#
2	28			2	434	1	X	2	840			2	1246	15		2	1652			2	2058	14		2	2464			2	2870	13		2	3276			2	3682	12		2	4088		
3	42	2		3	448			3	854	1	X	3	1260			3	1666	15		3	2072			3	2478	14		3	2884			3	3290	13		3	3696			3	4102	12	
4	56			4	462	2		4	868			4	1274	1	X	4	1680			4	2086	15		4	2492			4	2898	14		4	3304			4	3710	13		4	4116		
5	70	3		5	476			5	882	2		5	1288			5	1694	1	X	5	2100			5	2506	15		5	2912			5	3318	14		5	3724			5	4130	13	
6	84			6	490	3		6	896			6	1302	2		6	1708			6	2114	1	X	6	2520			6	2926	15		6	3332			6	3738	14		6	4144		
7	98	4		7	504			7	910	3		7	1316			7	1722	2		7	2128			7	2534	1	X	7	2940			7	3346	15		7	3752			7	4158	14	
8	112		ϕ	8	518	4		8	924			8	1330	3		8	1736			8	2142	2		8	2548			8	2954	1	X	8	3360			8	3766	15		8	4172		
9	126	5		9	532			9	938	4		9	1344			9	1750	3		9	2156			9	2562	2		9	2968			9	3374	1	X	9	3780			9	4186	15	
10	140		Δ	10	546	5	Δ	10	952		Δ	10	1358	4	Δ	10	1764		Δ	10	2170	3	Δ	10	2576		▲	10	2982	2	Δ	10	3388		Δ	10	3794	1	XΔ●	10	4200		Δ
11	154	6	X	11	560			11	966	5		11	1372			11	1778	4		11	2184			11	2590	3		11	2996			11	3402	2		11	3808			11	4214	1	X
12	168			12	574	6	X	12	980			12	1386	5		12	1792			12	2198	4		12	2604			12	3010	3		12	3416			12	3822	2		12	4228		
13	182	7		13	588			13	994	6	X	13	1400			13	1806	5		13	2212			13	2618	4		13	3024			13	3430	3		13	3836			13	4242	2	
14	196			14	602	7		14	1008			14	1414	6	X	14	1820			14	2226	5		14	2632			14	3038	4		14	3444			14	3850	3		14	4256		
15	210	8		15	616			15	1022	7		15	1428			15	1834	6	X	15	2240			15	2646	5		15	3052			15	3458	4		15	3864			15	4270	3	
16	224			16	630	8		16	1036			16	1442	7		16	1848			16	2254	6	X	16	2660			16	3066	5		16	3472			16	3878	4		16	4284		
17	238	9		17	644			17	1050	8		17	1456			17	1862	7		17	2268			17	2674	6	X	17	3080			17	3486	5		17	3892			17	4298	4	
18	252			18	658	9		18	1064			18	1470	8		18	1876			18	2282	7		18	2688			18	3094	6	X	18	3500			18	3906	5		18	4312		
19	266	10		19	672			19	1078	9		19	1484			19	1890	8		19	2296			19	2702	7		19	3108			19	3514	6	X	19	3920			19	4326	5	
20	280			20	686	10		20	1092			20	1498	9		20	1904			20	2310	8		20	2716			20	3122	7		20	3528			20	3934	6	X	20	4340		
21	294	11	X	21	700			21	1106	10		21	1512			21	1918	9		21	2324			21	2730	8		21	3136			21	3542	7		21	3948			21	4354	6	X
22	308			22	714	11	X	22	1120			22	1526	10		22	1932			22	2338	9		22	2744			22	3150	8		22	3556			22	3962	7		22	4368		
23	322	12		23	728			23	1134	11	X	23	1540			23	1946	10		23	2352			23	2758	9		23	3164			23	3570	8		23	3976			23	4382	7	
24	336			24	742	12		24	1148			24	1554	11	X	24	1960			24	2366	10		24	2772			24	3178	9		24	3584			24	3990	8		24	4396		
25	350	13		25	756			25	1162	12		25	1568			25	1974	11	X	25	2380			25	2786	10		25	3192			25	3598	9		25	4004			25	4410	8	
26	364			26	770	13		26	1176			26	1582	12		26	1988			26	2394	11	X	26	2800			26	3206	10		26	3612			26	4018	9		26	4424		
27	378	14		27	784			27	1190	13		27	1596			27	2002	12		27	2408			27	2814	11	X	27	3220			27	3626	10		27	4032			27	4438	9	
28	392			28	798	14		28	1204			28	1610	13		28	2016			28	2422	12		28	2828			28	3234	11	X	28	3640			28	4046	10		28	4452		
29	406	15		29	812			29	1218	14		29	1624			29	2030	13		29	2436			29	2842	12		29	3248			29	3654	11	X	29	4060			29	4466	10	

KEY: A - MCAI SCANS LOW-SPEED CHANNEL
B - TIME IN MICROSECONDS
C - PCR SCANS HIGH-SPEED CHANNEL OR MCAI

O - MCAI SCANS LOW-SPEED CHANNEL 1
X - PCR SCANS MCAI
- PCR & MCAI HAVE COINCIDENT SCANS ON CHANNEL 1
▲ DATA SAMPLE 6 TAKEN FROM LOW-SPEED CHANNEL 10 - TIMING BIT COMPLEMENTED

ϕ - DATA TRANSITION OCCURS ON LOW-SPEED CHANNEL 10
Δ - DATA SAMPLE TAKEN FROM LOW-SPEED CHANNEL 10
● - DATA BIT TRANSFERRED TO PCR - FROM MCAI FOR CHANNEL 10

ERROR CHECKING

A feedback loop from the communications channels to the MCA1 is provided to check for the correct transmission of data to the communication channel.

In send status when the MCA1 transfers a bit to a channel's output latch, the LDS bit is made to match the bit in the output latch. Checking for correct line transmission of the bit in the output latch is done just prior to changing the output latch for the next bit. The status of the LDS bit and the status of the sending channel fed back through the MCA1 input scanner are compared. If they do not compare, an error latch is set. This causes the MSDR data bit to be different than the last data bit transferred from the PCR. The PCR will detect this difference as an error during the next coincident scan in which a timing line reversal has been detected and activate its error circuitry.

This comparison gives an error check on the operation of transferring bits from the control storage distribution area to the MCA1 and subsequently to the communications channels. In addition, the operation of the input scanner is checked.

TYPE 2 HIGH SPEED CHANNEL ADAPTER

The Type 2 High Speed Channel Adapter (HSA2) adapts one or two 7750 scan points, depending on half duplex or full duplex service, to an IBM terminal provided with STR (Synchronous Transmitter Receiver), such as the IBM 7701 Magnetic Tape Transmission Terminal or the IBM 1009 Data Transmission Unit. The HSA2 requires no clocking information from the subset provided by the communications company and generates its own bit synchronization from a crystal controlled oscillator and bit clock which corrects its own strobe on received data. No character assembly is done by HSA2 as the data moving operation is serial by bit between the Process Control Rack and the Communications Line Terminator (CLT). HSA2 accepts bits from the Process Control Rack and transmits them through the CLT to the remote terminal. On receiving, HSA2 samples information serially to the Process Control Rack, Figure 21. HSA2 is capable of operating at 600 or 1200 bits per second. The operating speed of an HSA2 may be selected from the 7750 operator's panel subassembly by the customer. Each HSA2 may operate at either of the two speeds mentioned.

HSA2 may operate half duplex or full duplex. When operating half duplex HSA2 requires only one 7750 scan point. However, two scan points are required for full duplex operation -- one each for the send only and receive only channels. HSA2 may be changed from half duplex to full duplex.

HSA2 provides one bit buffering and speed changing between two interfaces in both directions. On the one side HSA2 exchanges information with the Process Control Rack via the Adapter Control Interface. On the other side HSA2 transmits or receives information to CLT which in turn relays this information to the communications line.

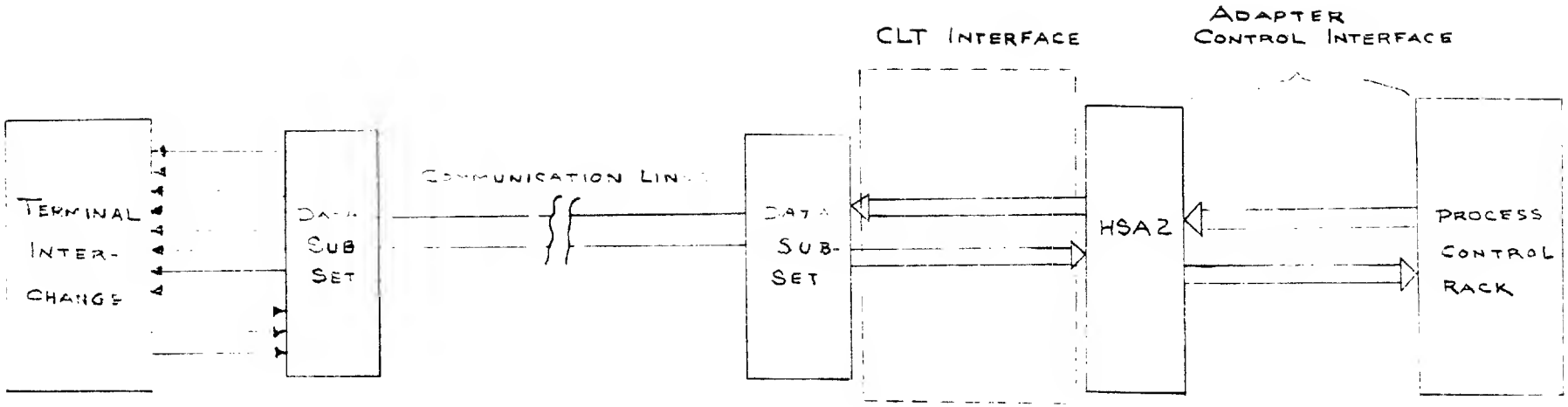


FIGURE 21 HSA2 CONNECTIONS

ACIF Operation

Each time the Process Control Rack Channel scanner is incremented a new select line is generated. This select line is said to come from one of the IBM 7750 Scan Points. When HSA2 becomes selected its seven bit Control Storage address is gated onto the ACIF. The Process Control Rack uses this address to access the channel word, CWD, for HSA2 from Control Storage. Once the CWD is in place in the CSDR a transfer of information occurs across the ACIF causing HSA2 and the Process Control Rack to take different actions. The Channel Word is written back into Control Storage and the channel scanner is incremented to the next scan point. During this select period the bits derived by HSA2 are transferred to the Process Control Rack or the next bit to be sent by HSA2 is transferred to HSA2 to be buffered until Transmit Strobe Time.

Transmitting

To transmit a message the programmer first sets up an output chain in Process Storage and moves the CWD to its proper location in Control Storage. The format of this CWD will be Synchronous Send described under Data Transfer Check. When HSA2 is selected it will raise the Request to Send linc of the CLT Interface and initialize the Timing and Data In lines of the ACIF in response to the Adapter Synchronization received on the ACIF. Timing changes will not be allowed until the Character Phase Counter counts through zero. The next time HSA2 is selected there will be a logical difference between the Timing line of ACIF and bit 31 of CSDR, last timing bit. On such a difference the Process Control Rack will transfer the next bit to be transmitted by HSA2 on line #2 or #3 depcnding on the logical value of the bit. HSA2 accepts this bit and buffers it until Transmit Strobe time when it is placed on the transmit data line of the CLT Interface for Transmission. At Transmit Strobe time the timing lines of ACIF is complemented and the logical value of the Transmit Data line is fed back to the Data In line of ACIF. The next time HSA2 is selected the Process Control Rack sees another change of the Timing Line and gates the next bit to be transmitted onto ACIF and checks the value of the Data In line with the previous bit sent to HSA2. If Data In does not agree with the last bit sent to HSA2, a Data Transfer Check occurs. This process continues until the last bit of the last character has been transferred to HSA2 via the ACIF when the Process Control Rack performs a character interrupt to get the next character to be sent. Following the last character to be sent, the programmer has placed the Status Change Character, SCC, and it is placed into the assembly area of the CWD as the next character to be sent. This is recognized by the Process Control Rack and preparations are made to turn the line around to receive. After sufficient time has elapsed for the last bit to be fully transmitted HSA2 is changed to receiving hunt status and an Adapter Synchronization is given to HSA2 via the ACIF. HSA2 is not in an inactive state.

This description holds for both full-duplex and half-duplex operation of HSA2 with the understanding that when the send only channel of HSA2 is placed in receiving hunt status on full-duplex,it is placed in an inactive state and is not capable of receiving data.

Reeeiving

When the IBM 7750 program is started the channel words are moved from Process Storage to Control Storage making the ehannels active. Normally the format of the CWD moved to the Control Storage loeation assigned to an HSA2 will be synchronous Reeeive. This word format will initially be set to reeeiving hunt. With the CWD in reeciving hunt the Proeess Control Raek will shift bits as they are transferred from HSA2 through the extended assembly area of the CSDR looking for the character sync pattern. HSA2, howcver, will not be transferring bits to the Process Control Rack until it starts recciving data through the CLT Interfaee. When data is reeeived from the communieations linc the Carrier On line of the CLT Interfaee becomes a logieal onc. This linc is then used as a logieal gate to start allowing ehanges to occur to the Timing line of ACIF at Reeeive Strobe time. At Receive Strobe time the Reeeive Data line of the CLT Interface is sampled and the bit derived is buffered in a lateh feeding thc Data In line of ACIF. The Timing line is also eomplemented at Reeeive Strobe time. When HSA2 is seleeted by the Proeess Control Rack channel scanner a difference occurs bctween the Timing line of ACIF and bit 31 of CSDR, Last Timing bit. The Proeess Control Raek knows from this differenee that a new bit has arrived on the Data In line and gates it into the Assembly Area of CSDR. Process Control Raek also updates thc value of bit 31 of CSDR to agrce with the Timing Line of ACIF so that the same bit will not bc sampled twiec. Bits arc transferred to the Proeess Control Rack in this mannor. When thc Charaetcr Sync pattern has been recognized by the Process Control Raek the CWD falls out of receiving hunt and starts eounting bits and moving assembled characters to the reeeiving ehain for the channel when the number of bits assembled equals the eharaeter length specified in the CWD.

Error Indieation

HSA2 is eapable of ealling program attention to two types of ehannel errors via a Service Mode requcst and interrupt of all lower priority modes. When indieating channel errors HSA2 will change two bits of the scven bit Control Storage address to which it is assigned in order to aeeess a Channel Word other than that used for normal operation. At the same time the Attention line of ACIF is brought to logieal one and the Error line of ACIF may or may not be brought to logical one depending on the type of error. The next time HSA2 is scleeted by the Proeess Control Raek channel scanner the Error Channel Word is read into the CSDR. The error is reeognized and service mode is requested. Also the address of the channel in error is moved to the ehannel service register for the program to interrogate. For details of this operation refer to the section on Channel Errors.

Interloek Error

The Interloek line of the CLT Interfaee is at logieal one whenever the subset at the local end of the communications line of HSA2 has power on and its logical circuits are

functioning properly. If this line should drop to a logical zero when the 7750 has power on, the Interlock Error will be signalled to the attention of the program. HSA2 places logical ones on both the Attention and Error lines of the ACIF. The channel check light associated with the scan point to which HSA2 is connected will be turned on by the Interlock Error.

Time-Out Tag for Half-Duplex HSA2

When HSA2 has completed transmission of a message to a remote terminal it will be placed in receiving hunt via the SCC, Status Change Character. From the time that HSA2 is placed in receive status to the time that the Process Control Rack recognizes the received character sync pattern and starts assembling characters and moving them to the receiving chain in Process Storage HSA2 is timing out. The duration of this time out cycle is three seconds. If the Process Control Rack has not recognized the character sync pattern and assembled at least one character before this time out cycle times out, a Time-Out Tag will be signalled to the attention of the program. However, if a character has been assembled before the time out cycle times out, HSA2 will receive logical ones on the Character Complete line of the ACIF each time a new character is assembled. HSA2 uses these logical ones to replace the hold of the time out cycle to prevent a time out.

The IBM 7750 program will use this Time-Out Tag as a signal that bit synchronization must be re-established with the remote terminal before proceeding with transmission.

Time-Out Tag for Full-Duplex HSA2

With full-duplex operation of HSA2, idle characters will always be received on the Receive Only channel when messages are not being received. When the 7750 sends a message on the Send Only channel to which it expects a reply a time limit for that reply is imposed by the hardware. This time limit is three seconds, the same limit as for Time-Out Tag on half-duplex. Again HSA2 has been given the responsibility for keeping track of this time.

When the programmer sets up his message to be transmitted by the 7750, he inserts as the last two characters of his message first an Action Delay Character, ADC, and then SCC. When the ADC is brought into the assembly area of the CSDR a new Y field is transferred to the channel word of the Send Only channel having the Not Control Bit, bit 13 of CSDR, set to a logical zero. Then SCC is brought into the channel word which makes the Send Only channel inactive. The Not Control Bit of CSDR being at logical zero sets the Control Line of the ACIF to a logical zero. HSA2 interprets logical zero on the Control Line as a signal to start a three second time out cycle. If the Control Line of the ACIF is not replaced to a logical one before three second elapses, a Time-Out Tag will be signalled to the attention of the program. However, if the Not Control Bit of the Channel Word had been restored to logical one by the program before three

second elapses, HSA2 will receive logical ones on the Control Line of ACIF each time it is selected. HSA2 uses these logical ones to prevent the three second time out cycle from timing out. The Not Control Bit of CSDR is restored to a logical one by the program when it detects the reply expected. This reply may be inserted in the middle of another record being received.

The IBM 7750 program will use this Time-Out Tag as a signal that an Inquiry must be sent to the remote terminal asking for the reply to the transmitted record.

Control Storage Address Assignments

Each HSA2 requires 3 or 4 sequential addresses in Control Storage depending on whether HSA2 is operating half-duplex or full-duplex, respectively. Assignment of Control Storage Words is made according to Table 11. This assignment depends on the customer's Channel Adapter Rack configuration. This section will only describe the arrangement within the sequential block assigned to an HSA2 of the normal channel word and error channel words. For either half-duplex or full-duplex there may be either a horizontal or vertical assignment of words to HSA2.

Half-Duplex Vertical Assignment:

-----00 is assigned to the normal CWD.
-----01 is assigned to the error CWD for Interlock Error.
-----10 is assigned to the error CWD for Time-Out Tag.

Half-Duplex Horizontal Assignment:

00-----is assigned to the normal CWD.
01-----is assigned to the error CWD for Interlock Error.
10-----is assigned to the error CWD for Time-Out Tag.

Full-Duplex Vertical Assignment:

-----00 is assigned to the Receive only CWD.
-----01 is assigned to the error CWD for Interlock Error.
-----10 is assigned to the Send only CWD.
-----11 is assigned to the error CWD for Time-Out Tag.

Full-Duplex Horizontal Assignment:

00-----is assigned to the Receive only CWD.
01-----is assigned to the error CWD for Interlock Error.
10-----is assigned to the Send only CWD.
11-----is assigned to the error CWD for Time-Out Tag.

In this discussion address bits represented by (-) are fixed and equal for each word address assigned to a particular HSA2.

Operator's Switches and Data Lights

The Operator's Panel sub-assembly contains four sets of data lights and four rotary speed select switches. Each set of data lights indicate the six lines of the CLT interface. The operator can see at a glance the state of any HSA2 of four indicated on the sub-assembly. The operator may also change the operating speed of any of four HSA2 in accordance with the speed of operation on the communication line.

FM-STR Distortion

For FM-STR operations, the receiving distortion is the absolute difference between a consecutive marking bit and a spacing bit (or spacing bit and marking bit) divided by four normal bit periods. This ratio is expressed as a percentage.

Example: Two consecutive bits are found where the marking (space) bit is 750 us and the space (marking) bit is 250 us where a normal bit is 500 us (2000 bits/sec.). The distortion is:

$$D = \frac{750 - 250}{4\ (500)} = 0.25 = 25\%$$

Distortion discussed does not include the effects of speed variation or drift between the controlling oscillators at each end of the communications facility. This is a separate subject that will be considered by itself.

Once bit synchronization has been established, distortion can be increased gradually and the STR clock will maintain the bit synchronization. However, if this highly distorted signal were transmitted to a clock not in bit synchronization it might possibly never synchronize. Therefore the limiting point for distortion is that limit beyond which bit synchronization will not be established.

In operation with the STR, it is the Idle character that is used to establish bit synchronization and hence character phase. This Idle character is of the form -- Mark, Space, Space, 3 Marks, Space, Space. It is the two space bits in this character that allows synchronization to be established with a distorted signal. Synchronization can be established and maintained receiving Idle characters with up to 25% distortion. With over 25% distortion the HSA2 bit clock will start sampling the distorted bit twice -- deriving false information. With exactly 25% distortion, reliable operation cannot be guaranteed.

COMMUNICATIONS LINES TERMINATOR

The Communications Line Terminator connects common carrier equipment to the 7750. It changes common carrier voltage levels to those used in IBM circuits and changes IBM voltage levels to those used in communication channels. In addition to the CLT, another module, called the Telephone Line Adapter, may be obtained as an optional feature. This module contains equipment to convert IBM signal levels to certain

telegraph signal levels. To perform these functions efficiently, the CLT:

a. Provides a standardized interface to the common carrier.

b. Is capable of switching off line to permit testing the processor without disturbing the communication lines.

c. Permits customer reassignment of channels for service fault location.

d. Permits customer selection and speed control of an extra low speed channel for fault location or temporary usage.

e. Facilitates a diagnostic wrap-around of the entire machine under one control including the necessary line isolation.

f. Provides a test pattern generator including the necessary timing pulses for use in testing individual high speed lines.

General Characteristics

The CLT is physically attached to the I-O frame of the 7750 and is connected externally to the 7750 by cable. The unit consists of one rack and panel type module with appropriate covers and associated hardware. It handles low speed lines at transistor levels. When the low speed lines are handled at relay levels, an additional rack and panel type frame (Telegraph Line Adapter) is required. It is connected to the Basic CLT unit with 10 feet of cable and contains the relays necessary for this operation.

1. Low Speed Line Termination -- The CLT can terminate a maximum of 112 lines at speeds up to 200 bps. When a Telegraph Line Adapter is used with the CLT, maximum line speed is 75 bits per second. The lines are half duplex consisting of one send circuit, one receive circuit, one signal ground and one frame ground for each low speed communication line.

2. High Speed Line Termination -- The CLT can operate with any high speed data subset of 1,200 bits per second or less and conform to EIA Standard No. 232.

3. Off line and Diagnostic Status -- All high and low speed channels can be functionally disconnected from the communication lines and subsets by depressing the wrap-around switch. When in the off line status, the send circuits of the off numbered channels are connected to the receive circuits of the next higher order channels to effect a paired wrap-around of two adjacent like channels for diagnostic test purposes. The wrap-around of the adjacent like channels will cause an echo to be simulated on each low speed line. Depressing the simulation switch causes a test pattern to be generated for testing individual high speed channels.

Customer Facilities

The CLT has a patchboard whereby the customer can alter the line to channel assignment. This permits the customer to localize a trouble fault, i.e., IBM equipment or common carrier.

Low Speed Patchboard

The low speed patchboard has a two-circuit-line jack and a two-circuit-channel jack. The line jack refers to the common carrier and the channel jack refers to the 7750. The two jacks are internally connected in such a way that no plug is needed in either jack. Line No. 1 is connected with channel No. 1, line 2 is connected to channel 2, and so on. Therefore, under normal operating conditions, no patch cores are plugged into any of the jacks.

High Speed Patchboard

The high speed patchboard has two multi-pin connectors. One connection refers to the common carrier and the other refers to the 7750. Connection between the two is established by a multi-wire patch cord. This patch cord must be externally connected by the customer for the high speed circuits to be operational.

Low Speed Test Channels

One low speed test channel is provided for each M.C.A. group specified in the 7750. By using this switch, the customer can select the speed of the test channel to match the speed of the line to which the test channel is patched.

Effect of Patchboard on Programming

If any change is made in the patchboard, the program must be altered to reflect the change. This applies to a diagnostic wrap-around as well as on line.

Diagnostic Facilities

Sense Lines

The CLT contains five sense lines. These lines, controlled by the computer, perform the following functions:

a. Simulate carrier failure
b. Restore carrier or interlock
c. Simulate interlock failure
d. Master Reset
e. Simulate echo failure

Lines a, b, and c are used in diagnostic programming to simulate high speed subset carrier or interlock failures. Lines d and e are used to control echo checks on the low speed circuits during transmit. All of the above sense instructions are operable only when in the wrap-around status.

Clocking for High Speed Channels

In off line status or wrap-around condition, 2,000 bps clocking (for test purposes only) is provided for all high speed channels. This clocking is used by those channels which require clocking from the subset, but is ignored by those channels not requiring clocking from the subset.

LOW SPEED OPERATION (ON LINE)

In the event that trouble is experienced on a low speed line, the customer can perform the following tests:

a. Cross the line channel assignment; plug line 1 to Channel 2, line 2 to Channel 1 and so on. Any crossing assignment may be made as long as line and Channel speeds are matched. From the result, the customer can predict whether the common carrier line or IBM Channel is at fault.

b. Patch the faulty line into an unused channel of the same speed. From the results he can predict the source of trouble.

c. Patch the faulty line into a test channel. The speed of the test channel can be adjusted by a switch to match the line speed. From these results he can also predict the source of the trouble. If the trouble was in a channel rather than in a line, the customer can continue operation temporarily using the test channel.

d. Wrap any two channels, including the test channel with a special patch cable.

HIGH SPEED OPERATION (ON LINE)

Any two channel combinations may be crossed and analyzed in a manner similar to that described for low speed operation.

DIAGNOSTIC OPERATION (OFF LINE)

Low Speed Wrap-Around

The wrap-around switch, when ON, causes an echo to be generated for each low speed transmission channel. The diagnostic program transmits on a channel and receives on

the paired channel. The program can compare the transmitted data and the received data to verify the operation. It must be noted that if any patching appears in the patch panel, it will alter the wrap-around combinations.

Low Speed Sense Line Control

The diagnostic program can impulse sense line e and thus inhibits the echo. The program can then transmit on each channel and expect to get an echo failure on each channel. The echo can subsequently be uninhibited by pulsing the master reset sense line. Whenever sense lines d or e are pulses, a 10 millisecond delay is required before thc next transfer of data.

High Speed Wrap-Around

High speed wrap-around is performed in the same manner as low speed. It is necessary that the patchboard configuration be recognized.

High Speed Sense Line Control

Scnse line (a) can bc pulsed to simulate a carrier failure and sense line (e) can be pulsed to simulatc an intcrlock failure. Sense line (b) can be pulsed to restore these two lines to their normal status.

Sense Line Timing

All sense lines will perform properly on a pulse of 20 microseconds. The resultant functions are operative only when the unit is in off line status.

The Channel Adapter Rack of the 7750 has been designed to be extremely modular, so that the system designer can be quite flexible in his choice of a communications network. However, certain limitations do exist in the choice of channel adapter configurations, and the purpose of this section is to point these out.

PROCESSING CAPABILITY

Processing capabilities must be carefully considered when designing a system employing the 7750. Under certain circumstances it may be possible to accept more characters from the communications network, than the 7750 can process. For example, sixteen high speed lines receiving six bit characters at the rate of 1200 bits per second per line will put into the 7750 about 3200 characters per second. Experience has shown, however, that a typical processing job requires about 15 instructions per character, causing Process Storage to overflow. If a relatively complex editing job is to be done on the incoming messages, through-put will be reduced. Therefore, do not assume that the 7750 is capable of processing a given number of characters just because the scanning mechanism is capable of receiving them. The details of the processing task, as well as the peak loading of the communications system, and the duration of this peak must be carefully examined. The system designer cannot be sure that the 7750 has enough processing power for a job until these factors are known.

Channel Capabilities

Certain requirements must be met when using the 7750 Channel Adapter rack. These are:

1. Packaging Requirements
2. Utilization of Process Control scan points.
3. Utilization of Control Storage Words.

Packaging Requirements

The 7750 Channel Adapter rack contains a maximum of four 10 x 28 SMS card panels. Each variety of channel adapter requires one or more panels in the Channel Adapter. The panels may be mixed in a variety of ways to match system requirements. Table 8 shows the packaging configurations of the various channel adapters.

Utilization of Process Control Scan Points

There are a total of 16 Process Control scan points which can be utilized by the Channel Adapters as shown in Table 9. Note that each MCA may be connected to

Type of Adapter	Type & Number of Lines	Number of Panels	Permissable Mounting Locations
MCA	0-56 Half Duplex	2	3 and 4
MCA	57-112 Half Duplex	3	1, 3 and 4
FM-STR	1 through 4 Half Duplex or 1 through 4 Full Duplex or Any combination of half and full duplex channels which total to four or less	1	1 or 2 or 3 or 4

TABLE 8

different numbers of scan points. The proper number to use is determined by the bit speed on the channels connected to the MCA. See Section on Input Bit Rates.

Utilization of Control Storage Words

Systems must not be designed which will use more space in Control Storage than is available. Eight words are required to run programs. The remaining 120 words may be assigned as channel words, with certain restrictions. Table 10 shows the number of Channel Words, and their function, required for each type of adapter.

The location of these words in Control Storage must be done in a specified manner. The Process Control rack uses address 31, 63, 94, 95, 126, 127 (decimal) for process words. MCA's will be assigned blocks of Control Storage, starting with address 0, 32, 64 and 96 (decimal). Addresses 28, 60, 92 and 124 (decimal) are reserved for test channels. When four MCA's are used, high speed adapters will be assigned blocks of four address, the low order five bits of which are constant, while the two high order bits change. Table 11 shows, as an example, how Control Storage Addresses would be assigned when four MCA's, each scanning 25 channels, and three high speed adapters are used.

When less than four MCA's are used, high speed adapters are assigned blocks of four addresses, the high order five bits of which do not change, while the low order two bits do change. As an example, Table 12 shows the case in which two MCA's, each scanning 29 channels, and eight, half duplex high speed adapters are used.

Input Bit Rates

The specifications in this section insure only that the 7750 will be able to get a bit from the communications channel. It does not insure that the processing capability of the 7750 is adequate to manipulate the total number of bits being received, or that information will not be lost due to too frequent demands for channel service.

Also, the bit rates given in this section do not include the effects of distortion. In many cases, the bit rates given assume perfect bit shapes. If distortion shortens a bit, the equivalent bit rate is raised. For example, consider a transmission rate of 100 bits per second, subject to 10% distortion which may shorten the bit. The minimum bit length is 9 milliseconds, corresponding to an equivalent bit rate of 111 bits per second. All bit rates given will still apply if the only effect of distortion is to lengthen the bit.

The 7750 is designed so that the Process Control scanner must scan every communication channel at least once during each bit time on that channel. Additionally, the MCA must take a certain minimum number of scans per bit time on each channel. These requirements may be broken down into two cases, high speed adapters and the MCA. For both cases certain terms will be defined:

H = total number of process control rack scan points used for all adapters.
L = number of low speed channels connected to an MCA, including the Test Channel.
N = number of main frame scan points connected to an MCA.

Type of Adapter	Number of Main Frame Scan Points Required
MCA	1 or 2 or 3 or 4
FM-STR Full Duplex	2
FM-STR Half Duplex	1

TABLE 9

Type of Adapter	Number of Channel Words Required	Purpose of Channel Words
MCA	One for each simplex channel connected to each MCA	Send or Receive
	One for each half-duplex channel connected to each MCA	Send or Receive
	Two for each full-duplex channel connected to each MCA	Send or Receive
FM-STR Full Duplex	Four	1. Receive 2. Send 3. Interlock Error 4. Time Out Tag
FM-STR Half Duplex	Three	1. Send or Receive 2. Interlock Error 3. Time Out Tag

TABLE 10

CONTROL STORAGE WORD REQUIREMENTS

Multiplexing Channel Adapter

The Multiplexing Channel Adapter will operate with a variety of bit rates, generally at 200 bits per second or less. Regardless of the operating speed, certain fundamental requirements must be specified.

These are:

A. Each MCA must scan an odd number of lines. The quantities, H and L, must contain no common factors.

B. Each MCA in an I-O frame must scan the same number of lines. This may mean scanning unused points in some MCA's.

C. Up to seven different bit rates may be used in one MCA. These speeds are assigned in groups of four channels. Scanning conditions which insure that the highest bit rate will be properly scanned, insure that all lower bit rates will also be properly scanned.

D. Each MCA may be connected to 1, 2, 3, or 4 main frame scan points. The more main frame scan points are used, the higher the bit rate that can be scanned in the MCA.

When these requirements are met, Tables 13 and 14 give the maximum bit rates which may be scanned with various numbers of main frame scan points, and various numbers of MCA scan points. These tables show the bit rates when an MCA is connected to one, two, three, or four main frame scan points.

In order to obtain the bit rates shown in Tables 15, 16, and 17 the main frame scan points to which the MCA is connected cannot be arbitrarily chosen. In general, certain combinations of scan points must be used. Tables 15, 16, and 17 show the proper combination of scan points for various numbers of MCA scan points and main frame scan points. In some cases, more than one combination of scan points will give equivalent results. In all cases, the starting point of the combination has been referred to scan point one. This represents an arbitrary reference point. For example, the combination 1-5-9 is equivalent to 2-6-10, or 5-9-13.

CONTROL WORD ASSIGNMENT CHART

	MCA-A		MCA-B		MCA-C		MCA-D	
0.	00---00	32.	00---00	64.	10---00	96.	11---00	
1.	00---01	33.	01---01	65.	10---01	97.	11---01	
2.	00---10	34.	01---10	66.	10---10	98.	11---10	
3.	00---11	35.	01---11	67.	10---11	99.	11---11	
4.	00---00	36.	01---00	68.	10---00	100.	11---00	
5.	00---01	37.	01---01	69.	10---01	101.	11---01	
6.	00---10	38.	01---10	70.	10---10	102.	11---10	
7.	00---11	39.	01---11	71.	10---11	103.	11---11	
8.	00---00	40.	01---00	72.	10---00	104.	11---00	
9.	00---01	41.	01---01	73.	10---01	105.	11---01	
10.	00---10	42.	01---10	74.	10---10	106.	11---10	
11.	00---11	43.	01---11	75.	10---11	107.	11---11	
12.	00---00	44.	01---00	76.	10---00	108.	11---00	
13.	00---01	45.	01---01	77.	10---01	109.	11---01	
14.	00---10	46.	01---10	78.	10---10	110.	11---10	
15.	00---11	47.	01---11	79.	10---11	111.	11---11	
16.	00---00	48.	01---00	80.	10---00	112.	11---00	
17.	00---01	49.	01---01	81.	10---01	113.	11---01	
18.	00---10	50.	01---10	82.	10---10	114.	11---10	
19.	00---11	51.	01---11	83.	10---11	115.	11---11	
20.	00---00	52.	01---00	84.	10---00	116.	11---00	
21.	00---01	53.	01---01	85.	10---01	117.	11---01	
22.	00---10	54.	01---10	86.	10---10	118.	11---10	
23.	00---11	55.	01---11	87.	10---11	119.	11---11	
24.	00---00	56.	01---00	88.	10---00	120.	11---00	
25.	00---01	57.	01---01	89.	10---01	121.	11---01	
26.	00---10	58.	01---10	90.	10---10	122.	11---10	HSA A 3
27.	00---11	59.	01---11	91.	10---11	123.	11---11	HSA A 2
28.	00---00	60.	01---00	92.	10---00	124.	11---00	
29.	00---01	61.	01---01	93.	10---01	125.	11---01	HSA A 1
30.	00---10	62.	01---10	94.	P.W.	126.	P.W.	
31.	P.W.	63.	P.W.	95.	P.W.	127.	P.W.	

TABLE 11

CONTROL WORD ASSIGNMENT CHART

	MCA		MCA-B				
0.	00---00	32.	01---00	64.	10---00 HSA	96.	11---00 HSA
1.	00---01	33.	01---01	65.	10---01	97.	11---01
2.	00---10	34.	01---10	66.	10---10 B-4	98.	11---10 A-1
3.	00---11	35.	01---11	67.	10---11	99.	11---11
4.	00---00	36.	01---00	68.	10---00	100.	11---00 HSA
5.	00---01	37.	01---01	69.	10---01	101.	11---01
6.	00---10	38.	01---10	70.	10---10	102.	11---10 A-2
7.	00---11	39.	01---11	71.	10---11	103.	11---11
8.	00---00	40.	01---00	72.	10---00	104.	11---00
9.	00---01	41.	01---01	73.	10---01	105.	11---01 HSA
10.	00---10	42.	01---10	74.	10---10	106.	11---10 A-3
11.	00---11	43.	01---11	75.	10---11	107.	11---11
12.	00---00	44.	01---00	76.	10---00	108.	11---00
13.	00---01	45.	01---01	77.	10---01	109.	11---01
14.	00---10	46.	01---10	78.	10---10	110.	11---10 HSA
15.	00---11	47.	01---11	79.	10---11	111.	11---11 A-14
16.	00---00	48.	01---00	80.	10---00	112.	11---00
17.	00---01	49.	01---01	81.	10---01	113.	11---01
18.	00---10	50.	01---10	82.	10---10	114.	11---10 HSA
19.	00---11	51.	01---11	83.	10---11	115.	11---11 B-1
20.	00---00	52.	01---00	84.	10---00	116.	11---00
21.	00---01	53.	01---01	85.	10---01	117.	11---01
22.	00---10	54.	01---10	86.	10---10	118.	11---10 HSA
23.	00---11	55.	01---11	87.	10---11	119.	11---11 B-2
24.	00---00	56.	01---00	88.	10---00	120.	11---00
25.	00---01	57.	01---01	89.	10---01	121.	11---01 HSA
26.	00---10	58.	01---10	90.	10---10	122.	11---10 B-3
27.	00---11	59.	01---11	91.	10---11	123.	11---11
28.	00---00	60.	01---00	92.	10---00	124.	11---00
29.	00---01	61.	01---01	93.	10---01	125.	11---01
30.	00---10	62.	01---10	94.	P.W.	126.	P.W.
31.	P.W.	63.	P.W.	95.	P.W.	127.	P.W.

TABLE 12

TABLE 13

Multiplexor Scanning Capabilities Where a Low Speed Group is Connected to One MF Scan Point

Number of MF Scan Points

Number of Low Speed Group Scan Points

D / E	1 b/s	2 b/s	3 b/s	4 b/s	5 b/s	6 b/s	7 b/s	8 b/s	9 b/s	10 b/s	11 b/s	12 b/s	13 b/s	14 b/s	15 b/s	16 b/s
1	All bit rates in this range are greater than 200 bits per second.													196	182	170
3													181	170	-	149
5											190	174	160	150	139	140
7										187	170	155	143	133	124	116
9										169	153	-	130	-	-	105
11								193	171	154	140	128	118	110	103	96
13								177	157	-	129	118	109	101	-	88
15							188	164	-	131	119	-	101	94	-	82
17							175	153	136	122	111	102	94	87	81	76

- indicates invalid combination

TABLE 14

Multiplexor Scanning Capabilities Where a Low Speed Group is Connected to Two MF Scan Points

Number of MF Scan Points

Number of Low Speed Group Scan Points (D / E)	1 To 11 b/s	12 b/s	13 b/s	14 b/s	15 b/s
To 21	All bit rates in this range are greater than 200 bps.				
23				193	193
25				---	177
27		188	188	---	164
29		175	175	153	153

--- indicates invalid combination

TABLE 15

Connection Points When an MCA is Connected to Two MF Scan Points

Number of MF Scan Points

Number of MCA Scan Points

H / L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	-	A	A	A	A	A	1,5	1,5	1,6	1,6	1,7	1,7	1,8	1,8	1,9	1,9
3	-	A	-	A	A	-	1,6	1,5	-	1,6	1,8	-	1,9	1,8	-	1,9
5	-	A	A	A	-	1,4	1,7	1,5	1,8	-	1,9	1,7	1,10	1,8	-	1,9
7	-	A	A	A	A	1,4	-	1,5	1,9	1,6	1,10	1,7	1,11	-	1,12	1,9
9	-	A	-	A	A	-	1,2	1,5	-	1,6	1,11	-	1,12	1,8	-	1,9
11	-	A	A	A	A	1,4	1,3	1,5	1,2	1,6	-	1,7	1,13	1,8	1,14	1,9
13	-	A	A	A	A	1,4	1,4	1,5	1,3	1,6	1,2	1,7	-	1,8	1,15	1,9
15	-	A	-	A	-	-	1,5	1,5	-	-	1,3	-	1,2	1,8	-	1,9
17	-	A	A	A	A	1,4	1,6	1,5	1,5	1,6	1,4	1,7	1,3	1,8	1,2	1,9
19	-	A	A	A	A	1,4	1,7	1,5	1,6	1,6	1,5	1,7	1,4	1,8	1,3	1,9
21	-	A	-	A	A	-	-	1,5	-	1,6	1,6	-	1,5	-	-	1,9
23	-	A	A	A	A	1,4	1,2	1,5	1,8	1,6	1,7	1,7	1,6	1,8	1,5	1,9
25	-	A	A	A	-	1,4	1,3	1,5	1,9	-	1,8	1,7	1,7	1,8	-	1,9
27	-	A	-	A	A	-	1,4	1,5	-	1,6	1,9	-	1,8	1,8	-	1,9
29	-	A	A	A	A	1,4	1,5	1,5	1,2	1,6	1,10	1,7	1,9	1,8	1,8	1,9

- indicates invalid combination

A indicates arbitrary connection

TABLE 16

Connection Points When an MCA is Connected to Three MF Scan Points

Number of MF Scan Points

H \ L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1			A	A	A	A	1-3-5 1-2-5	1, 4, 6	1, 4, 7	1-4-7 1-3-7	1, 4, 8	1, 5, 9	1-5-9 1-4-9	1, 6, 11	1, 6, 11	1-6-11 1-5-11
3			-	A	A	-	1-2-3 1-3-5	1, 2, 3	-	1-2-3 1-3-5	1, 2, 3	-	1-2-3 1-3-5	1, 2, 3	-	1-2-3 1-3-5
5			A	A	-	A	1-2-5 1-2-3	1, 2, 3	1, 4, 7	-	1, 3, 5	1, 5, 9	1-2-8 1-2-3	1, 4, 7	-	1-3-10 1-3-5
7			A	A	A	A	-	1, 4, 6	1, 4, 7	1-2-3 1-3-5	1, 2, 7	1, 5, 9	1-3-5 1-5-9	-	1, 6, 11	1-4-7 1-5-11
9			-	A	A	-	1-2-5 1-2-3	1, 4, 6	-	1-4-7 1-3-7	1, 4, 7	-	1-4-7 1-2-8	1, 4, 7	-	1-4-7 1-5-11
11			A	A	A	A	1-2-3 1-3-5	1, 2, 3	1, 4, 7	1-4-7 1-3-7	-	1, 5, 9	1-4-9 1-4-7	1, 2, 3	1, 6, 11	1-3-10 1-3-5
13			A	A	A	A	1-3-5 1-2-5	1, 2, 3	1, 4, 7	1-2-3 1-3-5	1, 4, 7	1, 5, 9	-	1, 5, 10	1, 6, 11	1-2-3 1-3-5
15			-	A	-	-	A	1, 4, 6	-	-	1, 2, 7	-	1-4-9 1-4-7	1, 5, 10	-	1-6-11 1-5-11
17			A	A	A	A	1-2-3 1-3-5	1, 4, 6	1, 4, 7	1-2-3 1-3-5	1, 4, 7	1, 5, 9	1-3-5 1-2-8	1, 2, 3	1, 6, 11	1-6-11 1-5-11
19			A	A	A	A	1-2-5 1-2-3	1, 2, 3	1, 4, 7	1-4-7 1-3-7	1, 2, 3	1, 5, 9	1-3-5 1-5-9	1, 4, 7	1, 6, 11	1-2-3 1-3-5
21			-	A	A	-	-	1, 2, 3	-	1-4-7 1-3-7	1, 4, 8	-	1-2-8 1-2-3	-	-	1-3-10 1-3-5
23			A	A	-	A	1-2-5 1-2-3	1, 4, 6	1, 4, 7	1-2-3 1-3-5	1, 4, 8	1, 5, 9	1-2-3 1-3-5	1, 4, 7	1, 6, 11	1-4-7 1-5-11
25			A	A	-	A	1-2-3 1-3-5	1, 4, 6	1, 4, 7	-	1, 2, 3	1, 5, 9	1-5-9 1-4-9	1, 2, 3	-	1-4-7 1-5-11
27			-	A	A	-	1-3-5 1-2-5	1, 2, 3	-	1-2-3 1-3-5	1, 3, 5	-	1-5-9 1-4-9	1, 5, 10	-	1-3-10 1-3-5
29			A	A	A	A	A	1, 2, 3	1, 4, 7	1-4-7 1-3-7	1, 2, 7	1, 5, 9	1-2-3 1-3-5	1, 5, 10	1, 6, 11	1-2-3 1-3-5

Number of MCA Scan Points

- indicates invalid combination

A indicates arbitrary connection

TABLE 17

Connection Points When an MCA is Connected to Four MF Scan Points

Number of MF Scan Points

Number of MCA Scan Points (L \ H)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1				A	A	A	A	1,3,5,7	1-3-5-7 1-2-4-7 1-2-5-7	1,4,7,10 1,3,5,8 1,3,6,8	1,4,7,10	1,4,7,10	1-4-7-10 1-2-6-10 1-3-7-11 1-3-7-10	1-4-8-12 1-5-8-12 1-3-7-11	1,5,9,13	1,5,9,13
3				A	A	-	A	1,3,5,7	-	1,2,3,4 1,2,3,7 1,2,6,7	1,3,5,7	-	1-2-6-10 1-2-3-4 1-2-3-10 1-2-6-7	1-3-5-10 1-3-8-10 1-3-5-7	1,4,7,10	1,5,9,13
5				A	-	A	A	1,3,5,7	1-2-3-4 1-2-5-8 1-2-4-8	-	1,2,5,9	1,4,7,10	1-3-5-7 1-2-7-8 1-2-4-8 1-3-7-10	1-2-3-9 1-2-8-9 1-3-7-9	-	1,5,9,13
7				A	A	A	-	1,3,5,7	1-2-5-6 1-2-4-7 1-2-4-5	1,2,3,4 1,2,3,7 1,2,6,7	1,2,3,4	1,4,7,10	1-3-6-11 1-3-5-7 1-2-4-6 1-3-4-6	-	1,3,5,7	1,5,9,13
9				A	A	-	A	1,3,5,7	-	1,2,5,8 1,3,5,8 1,3,6,8	1,2,6,7	-	1-2-3-4 1-4-7-10 1-2-4-7 1-3-4-6	1-2-3-9 1-2-8-9 1-3-7-9	-	1,5,9,13
11				A	A	A	A	1,3,5,7	1-2-5-6 1-2-5-8 1-2-4-5	1,4,7,10 1,4,7,9 1,4,6,9	-	1,4,7,10	1-2-7-8 1-3-6-11 1-2-7-10 1-2-6-7	1-3-5-10 1-3-8-10 1-3-5-7	1,2,3,4	1,5,9,13

- indicates invalid combination

A indicates arbitrary connection

TABLE 17 (Continued

L \ H	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
13				A	A	A	A	1,3,5,7	1-2-3-4 1-2-4-7 1-2-4-8	1-2-3-4 1-2-3-7 1-2-6-7	1,2,6,7	1,4,7,10	-	1-4-7-11 1-4-8-11 1-3-7-11	1,2,8,9	1,5,9,13
15				A	-	-	A	1,3,5,7	-	-	1,2,3,4	-	1-2-7-8 1-3-6-11 1-2-6-9 1-2-6-7	1-4-8-12 1-5-8-12 1-3-4-11	-	1,5,9,13
17				A	A	A	A	1,3,5,7	1-3-5-7 1-2-5-8 1-2-5-7	1,2,3,4 1,2,3,7 1,2,6,7	1,2,5,9	1,4,7,10	1-2-3-4 1-4-7-10 1-4-6-7 1-3-4-6	1-3-5-10 1-3-8-10 1-3-5-7	1,2,8,9	1-5-4-13
19				A	A	A	A	1,3,5,7	1-3-5-7 1-2-4-7 1-2-5-7	1,2,5,8 1,3,5,8 1,3,6,8	1,3,5,7	1,4,7,10	1-3-6-11 1-3-5-7 1-3-5-6 1-3-4-6	1-2-3-9 1-2-8-9 1-3-7-9	1,2,3,4	1-5-9-13
21				A	A	-	-	1,3,5,7	-	1,4,7,10 1,4,7,9 1,4,6,9	1,3,6,9	-	1-3-5-7 1-2-7-8 1-3-4-10 1-3-7-10	-	-	1-5-4-13
23				A	A	A	A	1,3,5,7	1-2-3-4 1-2-5-8 1-2-4-8	1,2,3,4 1,2,3,7 1,2,6,7	1,4,7,10	1,4,7,10	1-2-6-10 1-2-3-4 1-2-3-7 1-2-6-7	1-2-3-9 1-2-8-9 1-3-7-9	1,3,5,7	1-5-9-13

- indicates invalid combination

A indicates arbitrary connection

Number of MCA Scan Points

TABLE 17 (Continued

Number of MCA Scan Points

L \ H	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
25				A	-	A	A	1,3,5,7	1-2-5-6 1-2-4-7 1-2-4-5	-	1,3,5,7	1,4,7,10	1-4-7-10 1-2-6-10 1-3-6-10 1-3-7-10	1-3-5-10 1-3-8-10 1-3-5-7	-	1-5-9-13
27				A	A	-	A	1,3,5,7	-	1,2,3,4 1,2,3,7 1,2,6,7	1,2,5,9	-	1-4-7-10 1-2-6-10 1-3-7-11 1-3-7-10	1-4-7-11 1-4-8-11 1-3-7-11	-	1-5-9-13
29				A	A	A	A	1,3,5,7	1-2-5-6 1-2-5-8 1-2-4-5	1,2,5,8 1,3,5,8 1,3,6,8	1,2,3,4	1,4,7,10	1-2-6-10 1-2-3-4 1-2-3-10 1-2-6-7	1-4-8-12 1-5-8-12 1-3-4-11	1,4,8,12	1-5-9-13

- indicates invalid combination

A indicates arbitraty connection